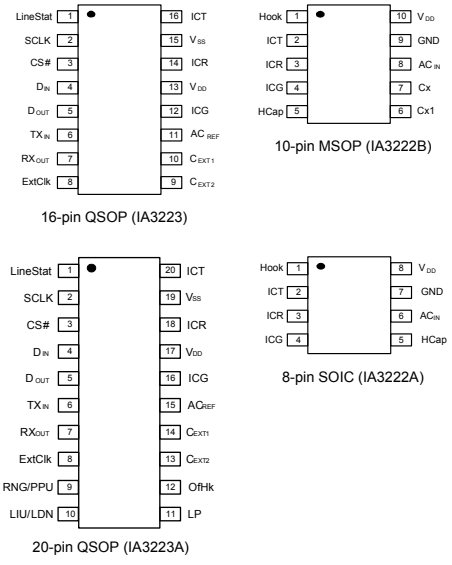
IA3222/IA3223 EZ DAA™ Chipset with Analog Interface

IA3222/IA3223

PACKAGE OPTIONS



16-pin QSOP (IA3223)

10-pin MSOP (IA3222B)

20-pin QSOP (IA3223A)

8-pin SOIC (IA3222A)

See back page for ordering information.

DESCRIPTION

The IA3222 and IA3223 integrated V.92 (56K) capable Data Access Arrangement (DAA) chipset is suitable for worldwide telephone line interface requirements and standards. The patented IsoBridge™ isolation technology eliminates the need for usual telecom isolation components, such as transformers or optocouplers. Innovative techniques reduce the overall number of discrete components, thus reducing the cost of the overall function.

The chipset can be programmed by software to pass PTT certification worldwide. The integrated V.92 EZ DAA™ offers an easy-to-use analog interface with an internal or external DC reference for interfacing to a variety of systems seamlessly. It allows easy building-block integration where audio codecs are either separate or integrated into DSPs. It is also ideal for non-modem systems requiring isolated DAAs, such as alarm systems, VoIP and PBX FXO interfaces, etc.

U.S. Patents #7,031,458 and #7,139,391

FEATURES

- Programmable worldwide telecom compliance with one hardware build
- V.92 (56kb/s) performance
- Virtually unlimited high-voltage isolation
- Highly competitive BOM cost
- Lowest pin count (26) chipset
- High common-mode RF immunity without costly filtering
- Continuous DC & audio snooping with >5MΩ Tip to Ring
- Parallel pick-up, line-in-use, ring, and "911" detection
- -86dBm receiver noise floor
- +6dBm transmit power
- Micropower line-side device powered from line
- 120dB Caller ID common-mode rejection at 120Hz

TYPICAL APPLICATIONS

- Fax-engine transformer DAA lower-cost retrofits
- Integrated modems
- Set-top boxes
- Point-of-sale terminals
- Metering devices
- Card readers
- Alarm systems
- PBX FXO/IP telephony

FUNCTIONAL BLOCK DIAGRAM

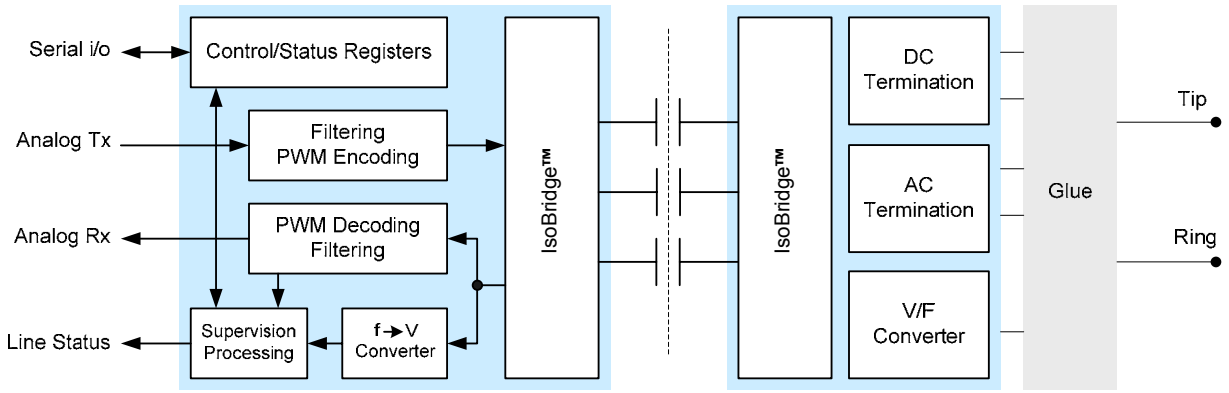


TABLE OF CONTENTS

TABLE OF FIGURES

OVERVIEW

The chipset provides, in an integrated solution, a low-cost worldwide compliant telephone line interface. Due to its high level of integration, only a few external components are required for operation. Its patented IsoBridge™ technology eliminates the need for costly and bulky transformers, yet still insuring a high level of isolation between the phone line and the system side.

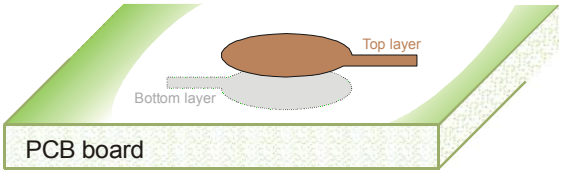
Analog Interface

The DAA is easily interfaced using single-ended transmitters and receivers. An extra input pin can be used to set the DC reference, thus facilitating the interfacing with or without coupling capacitors. Refer to the applications section below for more details.

Isolation Barrier

In most cases, equipment meant to be connected to the Public Switch Telephone Network must comply with specific safety requirements, including the implementation of a high-voltage isolation barrier between the telephone line side and the system side. Various standards require the isolation barrier to withstand from $1000V_{AC}$ to $3000V_{AC}$. The chipset implements a high-voltage isolation barrier between the IA3223 codec and its IA3222 line-side device by means of its patented IsoBridge technology. Where typical designs use costly transformers, optocouplers or discrete high voltage capacitors, IsoBridge reduces the Bill of Materials total cost by embedding high voltage capacitors into the PCB. This unique technique allows for virtually zero-cost capacitors.

PCB board material and thickness, trace width and pads dimensions determine the capacitance achieved by this technique. The IA3222/IA3223 requires three 0.7pF (nominal) capacitors to operate. The chipset is designed to operate over the wide variation range seen in standard PCB materials.



The application requires only three PCB capacitors, whose diameters range typically from 140 to 190 mils, depending on the thickness of the board.

International Compliance

The chipset can be programmed to meet all the variety of telecommunication requirements and standards worldwide through the serial loading of two registers.

Serial Interface

The IA3222/IA3223 can be programmed using a simple asynchronous serial protocol. Programming the DAA registers is asynchronous and independent of the data path.

When CS# is low (active), the first clock rising edge latches the read or write command. The next three clock edges latch a three-bit register address. The next four clock rising edges serially shift a four-bit data word in, or the next four clock falling edges serially shift a four-bit data word out, depending on the status of the read/write command. Refer to the timing diagrams in the specification section for more details on the serial interface.

International Programming Sequence

International programming options are loaded into the System Side and updated to the line side upon three possible events:

- Upon register loading if the line side is in the off-hook state
- When the line side is made to go off hook
- When the line side recovers from a line interruption

Hook control

The DAA is set on hook and off hook by writing a bit in a register through the serial interface.

Line Overload Protection

The chipset provides a built-in line-overload protection circuit to protect the IA3222 line-side device from unusual telephone line conditions, which could result in excessive voltage or current conditions. If the IA3222 senses an excessive line voltage (about 100V) when on hook, it will not go off hook even when an off-hook state is set in the control register. If the IA3222 senses an excessive loop current (about 170mA) when off hook, it will immediately go on hook. This will result in oscillation since in this case the IA3222 still sees an off-hook command and therefore keeps trying to go back off hook. While a fault condition exists, the LD status bit is high.

DC Termination (Voltage Drop vs. Loop Current)

The chipset offers four main DC termination modes and line-current limiting support specific for legacy TBR21 countries. Since TBR21 has been superseded by ES 203 021, European countries no longer rely on current limitation. While the IA3222/3223 chipset supports this mode for the few remaining countries that may still require current limiting, this requirement is expected to disappear rapidly. The four main DC headroom modes ensure that any country voltage-drop requirement can be met. The maximum transmitted level is different for each setting.

AC Termination (Line Impedance Matching)

The chipset offers several different AC impedance terminations selectable through the serial port. These AC impedances can be combined with any DC termination selected to address a country's loop or trunk interface requirements. Refer to the section "Return Loss and Trans-Hybrid Return Loss" for more details.

DTMF Dialing

DTMF dialing is synthesized and generated by the application; only a few parameters in the IA3223, such as the gain and maximum transmission level, need to be set prior to dialing.

Pulse Dialing

Pulse dialing is accomplished by going on hook and off hook repeatedly to generate the make and break pulses. It is the system application's responsibility to implement the different timings related to the pulse dialing specification, such as make/break times and ratio, inter-digit pause and pulses per second settings depending on the intended country 's specification. The IA3222 meets pulse-dialing overshoot requirements on inductive lines for Australia and a few other countries.

Caller ID

When the device is on hook, the Caller ID audio signal is available at the receiver output pin of the IA3223. This function is achieved while maintaining the high on-hook impedance required by telecom regulations. The gain can be set high (0 dB) for normal operation or low (-6 dB) for DTMF monitoring.

Power-Down Mode

In order to reduce power consumption, it is possible to set the IA3223 to power-down mode. In this state the device may not go off hook or monitor the line.

PACKAGE PIN DEFINITIONS

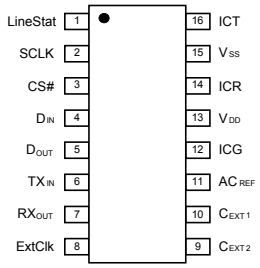
Pin-type key:

D=digital, A=analog, S=supply, I=input, O=output, IO=input/output

PU=weak internal pull-up resistor

PD=weak internal pull-down resistor

IA3223 System Side (QSOP-16)

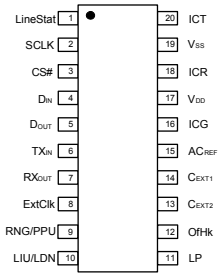


IA3223 System Side Pin Definitions

Pin Number	Pin Name	Pin Type	Pin Function
1	LineStat	DO, PU	Line Status open-drain output [See note.]
2	SCLK	DI	Serial interface clock
3	CS#	DI	Serial interface chip select, active low with weak pull-down
4	D_{IN}	DI	Serial interface data in
5	D_{OUT}	DO	Serial interface data out
6	TX_{IN}	AI	DAA transmit input
7	RX_{OUT}	AO	DAA receive output
8	ExtClk	DI, PD	Optional external clock; this pin may be left open.
9	C_{EXT2}	AIO	External capacitor #2 connection
10	C_{EXT1}	AIO	External capacitor #1 connection
11	AC_{REF}	AI	DAA optional DC offset; this pin may be left open.
12	ICG	AIO	Line-Side IsoBridge interface reference ground
13	V_{DD}	S	Positive power supply
14	ICR	AI	Line-Side IsoBridge interface for receiver path
15	V_{SS}	S	System ground
16	ICT	AO	Line-Side IsoBridge interface for transmitter path

Note: Refer to the section on line monitoring for a description of the Line-Status pin.

IA3223A System Side (QSOP-20)

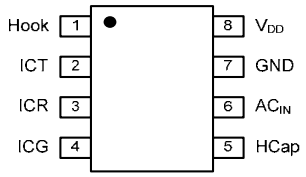


IA3223 System Side Pin Definitions

Pin Number	Pin Name	Pin Type	Pin Function
1	LineStat	DO, PU	Line Status open-drain output [See note.]
2	SCLK	DI	Serial interface clock
3	CS#	DI	Serial interface chip select, active low with weak pull-down
4	D_{IN}	DI	Serial interface data in
5	D_{OUT}	DO	Serial interface data out
6	TX_{IN}	AI	DAA transmit input
7	RX_{OUT}	AO	DAA receive output
8	ExtClk	DI, PD	Optional external clock; this pin may be left open.
9	RNG/PPU	DO	Ring signal (on hook) or parallel pickup (off hook)
10	LIU/LD	DO	Line in use or disconnect (on hook) or line drop (off hook)
11	LP	DO	Line polarity (on hook and off hook)
12	OfHk	DI, PD	Off hook, active high, ORed with internal OFH control bit
13	C_{EXT2}	AIO	External capacitor #2 connection
14	C_{EXT1}	AIO	External capacitor #1 connection
15	AC_{REF}	AI	DAA optional DC offset; this pin may be left open.
16	ICG	AIO	Line-Side IsoBridge interface reference ground
17	V_{DD}	S	Positive power supply
18	ICR	AI	Line-Side IsoBridge interface for receiver path
19	V_{SS}	S	System ground
20	ICT	AO	Line-Side IsoBridge interface for transmitter path

Note: Refer to the section on line monitoring for a description of the Line-Status pin.

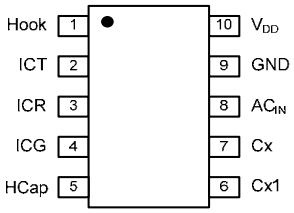
IA3222A Line Side (SOIC-8)



IA3222A Line Side Pin Definitions

Pin Number	Pin Name	Pin Function
1	Hook	Hook-switch control
2	ICT	Line-Side IsoBridge™ interface for transmitter path
3	ICR	Line-Side IsoBridge™ interface for receiver path
4	ICG	Line-Side IsoBridge™ interface reference ground
5	HCap	Holding capacitor connection
6	AC_{IN}	Receiver path sensing capacitor input
7	GND	Device ground
8	V_{DD}	Device supply, self regulated through hook-switch transistor

IA3222B Line Side (MSOP-10)



IA3222B Line Side Pin Definitions

Pin Number	Pin Name	Pin Function
1	Hook	Hook-switch control
2	ICT	Line-Side IsoBridge™ interface for transmitter path
3	ICR	Line-Side IsoBridge™ interface for receiver path
4	ICG	Line-Side IsoBridge™ interface reference ground
5	HCap	Holding capacitor connection
6	C_{X1}	Termination-impedance capacitor
7	C_X	Termination-impedance capacitor
8	AC_{IN}	Receiver path sensing capacitor input
9	GND	Device ground
10	V_{DD}	Device supply, self regulated through hook-switch transistor

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Junction operating and storage temperature	-40	150	ºC
ESD (human body model)		2	kV
Power-supply voltage	-0.5	7	V
Voltage at any pin	-0.5	V_{DD} + 0.5	V
Current at any input or output (System Side)	-100	100	mA
Loop Current (IA3222)		150	mA

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Operating temperature	-25		85	ºC
Vdd	Power-supply voltage	3.0	3.3	3.6	V
Vil	Logic low input voltage	0		35	% V_{DD}
Vih	Logic high input voltage	65		100	% V_{DD}
V_{ACREF}	Optional AC_{REF} pin reference voltage (see note)	1.2		1.8	V
	AC reference capacitor (pin left open — see note)		100		nF
C1	External capacitor #1		10		nF
C2	External capacitor #2		220		nF
	RX_{OUT} load resistance	2			kΩ
	RX_{OUT} load capacitance			200	pF
	Loop current	20		120	mA
	Loop current, degraded performance	14		130	mA
	Line voltage for Caller ID power	15		70	V
	Internal sampling rate based on external clock	57.6		83.333	kHz
tck	Serial clock period	25		∞	ns
tcssuf	Chip Select fall to clock rising edge setup time	12			ns
tcssur	Chip Select rise to clock rising edge setup time	12			ns
tcsh	Chip Select rise or fall to clock rising edge hold time	8			ns
tdisu	Data in to clock rising edge setup time	12			ns
tdih	Data in to clock rising edge hold time	8			ns
	IA3222 power derating over 25 ºC ambient		6		mW/ ºC

Note: The AC_{REF} pin may be left open, in which case this internal bias voltage needs to be decoupled to the audio ground by means of a 100nF capacitor. Refer to DC characteristics table for more information on driving the AC_{REF} pin.

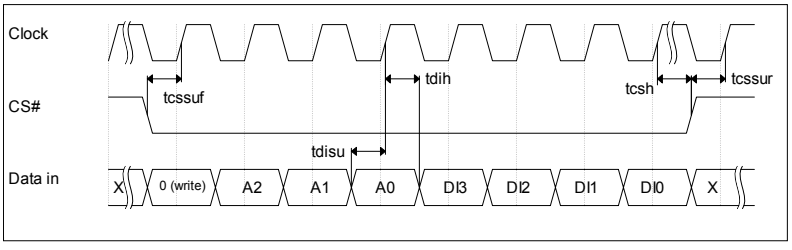


Figure 1: Serial interface write-cycle timing diagram (Data output pin floating)

DC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic input current		-10		10	µA
Logic input hysteresis			240		mV
Logic output low voltage	I_{OL} = -4mA			0.4	V
Logic output high voltage	I_{OH} = 4mA	0.8			V_{DD}
Ring-detection threshold	RTH[1:0] = 00	10		20	V_{RMS}
	RTH[1:0] = 01	12.5		25	V_{RMS}
	RTH[1:0] = 10	15		30	V_{RMS}
	RTH[1:0] = 11	20		40	V_{RMS}
Voltage at AC_{REF} pin	Pin left open	1.42	1.50	1.58	V
AC_{REF} input resistance	Small signal	42	60	78	kΩ
AC_{REF} input current	Sink or source		10		µA
Pull-down resistance	ExtClk, OfHk inputs, V = 0.65 Vdd	80		300	kΩ
Pull-up resistance	LineStat open-drain output, V = 0.35 Vdd	80		300	kΩ
Power supply current	Off hook, internal clock		7.9		mA
	Off hook, external clock		6.2		mA
	On hook		3.4		mA
	Power down, no external clock		2		µA
Loop-current sensor gain	Normal headroom, TBR21 mode		0.95		mV/mA
	All other headroom and impedance modes		1.15		mV/mA

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
tcdo	Clock falling edge to Data Out valid from driven or floating state		12	20	ns	Load = 50 pF
tcsdf	Chip Select disabled to Data Out floating		12	20	ns	Load = 50 pF
	Internal sampling rate based on internal clock	67.2	73.4	82.8	kHz	

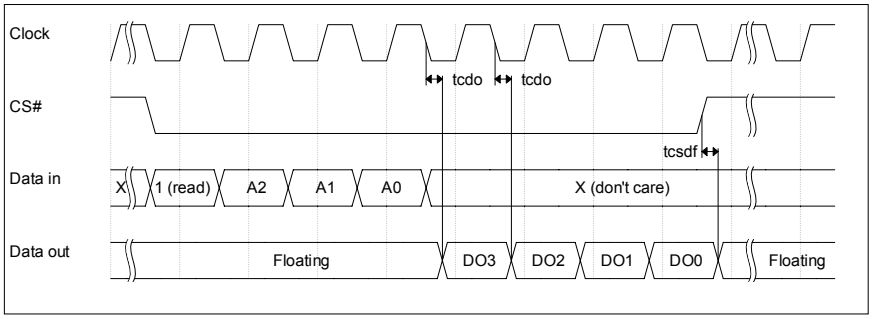


Figure 2: Serial interface read-cycle timing diagram

Off-Hook Receiver Performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Idle channel noise referred to Tip and Ring	300Hz - 3400Hz, 600 Ω, internal clock		-85		dBm
Total harmonic distortion	1kHz, -7 dBm, normal or high headroom		-76		dB
Gain from Tip and Ring to RX_{OUT} pin	1kHz (symmetrical around AC_{REF}), high headroom		-3		dB
Gain from Tip and Ring to RX_{OUT} pin	1kHz (symmetrical around AC_{REF}), other headrooms		0		dB
Receiver power headroom	Sine wave, high headroom, referenced to 600Ω	0			dBm
	Sine wave, normal headroom, referenced to 600Ω	-3			dBm
	Sine wave, low headroom, referenced to 600Ω	-3			dBm
	Sine wave, lowest headroom, referenced to 600Ω	-5			dBm
Maximum level at RX_{OUT} pin	1kHz (symmetrical around AC_{REF})		1.55		V_{PP}
Power-supply induced noise referred to Tip and Ring	1kHz, 100 mV_{PP} at V_{DD}, high headroom		-84		dBV
	1kHz, 100 mV_{PP} at V_{DD}, other headrooms		-87		dBV
	f > 3400Hz, DC coupled, high headroom		-66		dBV
	f > 3400Hz, DC coupled, other headrooms		-69		dBV
Longitudinal balance	f = 1000Hz		99		dB
Longitudinal balance	f = 3000Hz		93		dB

On-Hook Receiver (Caller ID) Performance at $48V_{DC}$

Parameter	Conditions	Min.	Typ.	Max.	Unit
Caller ID noise referred to Tip and Ring	400Hz - 3000Hz, internal clock		-48		dBV
Caller ID distortion	1kHz, 100 mV_{RMS}, normal or high headroom		-37		dB
Caller ID gain, Tip and Ring to AC_{REF}	1kHz, high gain setting		0.5		dB
	1kHz, low gain setting		-4.5		dB
Maximum level at Tip and Ring	1kHz, high gain setting		-3		dBm
	1kHz, low gain setting		+3		dBm
Maximum level at Rx pin	1kHz, high or low gain setting		1.55		V_{PP}
Power-supply induced noise referred to Tip and Ring	1kHz, 100 mV_{PP} at V_{DD}, high gain setting		-55		dBV
	1kHz, 100 mV_{PP} at V_{DD}, low gain setting		-50		dBV
Common-mode rejection	120Hz	120			dB

Transmitter Performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Idle channel noise referred to Tip and Ring	300Hz - 3400Hz, 600 Ω, internal clock		-82		dBm
Total harmonic distortion	1kHz, 3dB below clipping level, normal or high headroom		-78		dB
Gain from TX_{IN} pin to Tip and Ring	1kHz, 600 Ω, referenced to AC_{REF}, high headroom		9		dB
	1kHz, 600 Ω, referenced to AC_{REF}, other headrooms		6		dB
Part-to-part gain variation at 1kHz, 600 Ω mode, normal headroom	Transmitter gain		0.5		±dB
	Product of transmitter gain times receiver gain		0.5		±dB
Transmitter power headroom, sine wave (See note.)	LP[5:4]=00, 600Ω load	+6.5			dBm
	LP[5:4]=00, 900Ω load	+5.5			dBV
	LP[5:4]=01, 600Ω load	+3			dBm
	LP[5:4]=01, 900Ω load	+2			dBV
	LP[5:4]=01, Australia or TBR21 load	+2			dBV
	LP[5:4]=01, New Zealand load	+1			dBV
	LP[5:4]=10, 600Ω load, 400-3400 Hz	-5			dBm
	LP[5:4]=10, 600Ω load with bootstrap, 400-3400 Hz	-1			dBm
	LP[5:4]=11, 600Ω load, 400-3400 Hz	-9			dBm
	LP[5:4]=11, 600Ω load with bootstrap, 400-3400 Hz	-3			dBm
	LP[5:4]=11, 600Ω load with bootstrap, DTMF tones	-1			dBm
TX_{IN} pin input resistance		35	50	65	kΩ
Input common-mode rejection, defined as ($V(TX_{IN}) + V(AC_{REF})$) / 2	300Hz - 3400Hz, DC coupled		40		dB
	f > 3400Hz, DC coupled	40			dB
Power-supply induced noise referred to Tip and Ring (SGAIN = 0)	1kHz, 100 mV_{PP} at V_{DD}, high headroom		-86		dBV
	1kHz, 100 mV_{PP} at V_{DD}, other headrooms		-89		dBV
	f > 3400Hz, DC coupled, high headroom	-56			dBV
	f > 3400Hz, DC coupled, other headrooms	-59			dBV
Longitudinal balance	f = 1000Hz or f = 3000Hz	90			dB

Note: The bootstrap circuit shown in the application circuit (R18, C16 and Q6) is optional. Its function is to increase the transmit headroom voltage at the low and lowest headroom settings. Those settings should be used only when the DC voltage needs to be minimized for low-voltage countries such as Japan, Malaysia, etc.

Line-Side Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Self-regulated supply voltage			2.47		V
Current protection threshold		130	170	210	mA
On-hook voltage-protection threshold		80	108	135	V
Temperature-shutdown threshold	Loop current = 130 mA	136	146	156	ºC
On-hook DC resistance, Tip to Ring	5.6 MΩ voltage-sensing resistors	5			MΩ
Ringer equivalent load				0.1	REN
Return loss at 1 kHz (typical) or 300 – 3400 Hz (minimum)	600 Ω impedance mode and reference load	20	30		dB
	600 Ω + 1 µF impedance mode and reference load	20	30		dB
	900 Ω impedance mode and reference load	20	30		dB
	900 Ω + 1 µF impedance mode and reference load	20	30		dB
	Australia impedance mode and reference load	17	27		dB
	New Zealand impedance mode and reference load	20	26		dB
	TBR21 impedance mode and reference load	17	27		dB
Echo return loss, ITU-T G.122 method	600 Ω impedance mode and reference load	20	30		dB
	600 Ω + 1 µF impedance mode and reference load	20	30		dB
	900 Ω impedance mode and reference load	20	30		dB
	900 Ω + 1 µF impedance mode and reference load	20	28		dB
	Australia impedance mode and reference load	20	25		dB
	New Zealand impedance mode and reference load	20	26		dB
	TBR21 impedance mode and reference load	20	25		dB
Trans-hybrid distortion referred to line	600Ω load, -10 dBm signal, normal or high headroom		-91		dBm
Tip-Ring voltage	I_{DD} = 20mA, no current limit, lowest headroom		5.85	6	V
	I_{DD} = 20mA, no current limit, low headroom		6.4	7	V
	I_{DD} = 20mA, no current limit, normal headroom		7.8	9	V
	I_{DD} = 20mA, no current limit, high headroom		9	10	V
	I_{DD} = 42mA, TBR21 current limit, normal headroom			14.5	V
	I_{DD} = 50mA, TBR21 current limit, normal headroom			40	V
Loop-current limit	TBR21 legacy mode, 50 V, 230 Ω feed			60	mA

TYPICAL PERFORMANCE GRAPHS

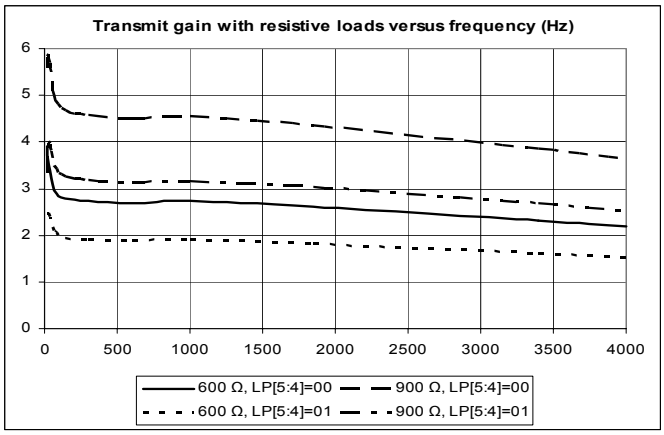


Figure 3: Transmit gain with resistive loads

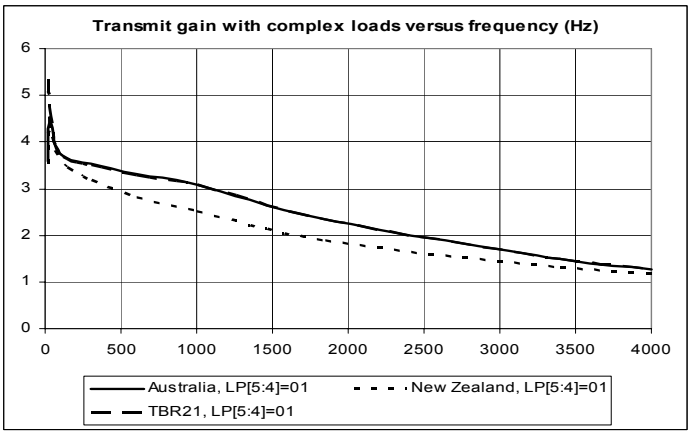


Figure 4: Transmit gain with complex loads

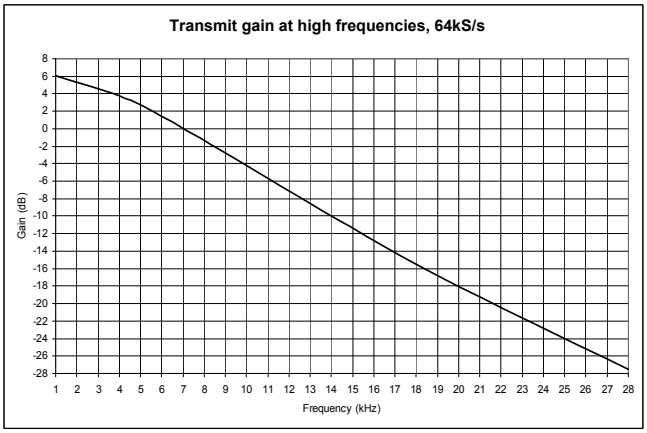


Figure 5: Transmit gain at high frequencies, 600 Ω

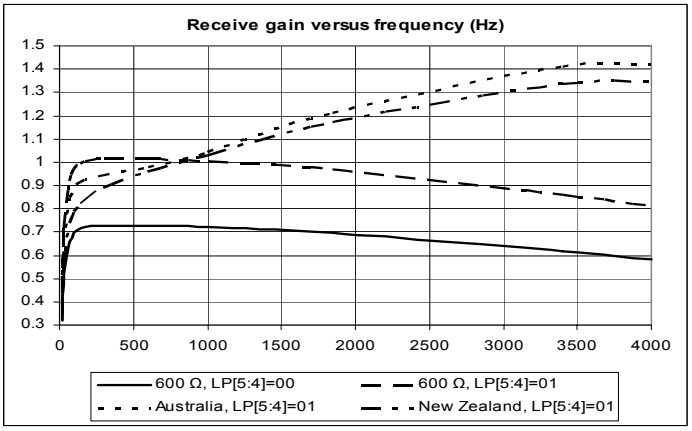


Figure 6: Receive gain versus frequency

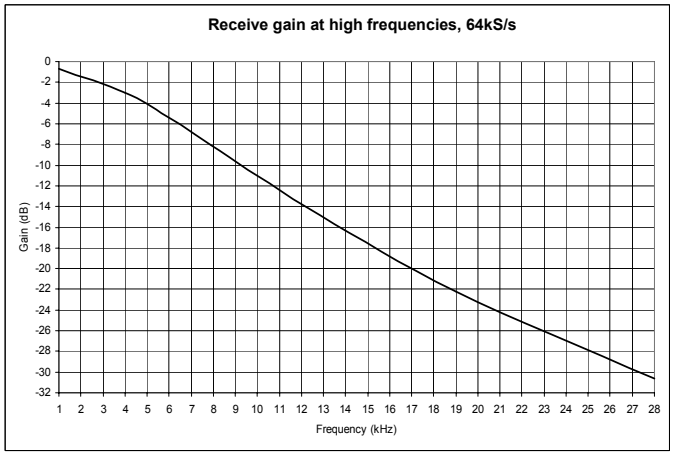


Figure 7: Receive gain at high frequencies, 600 Ω

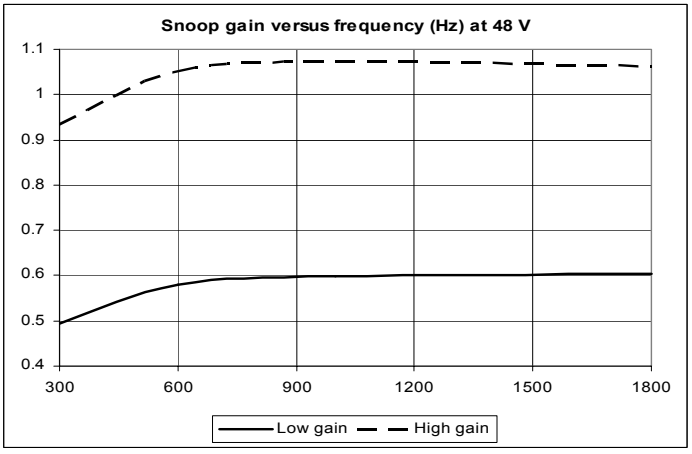


Figure 8: Snoop gain versus frequency

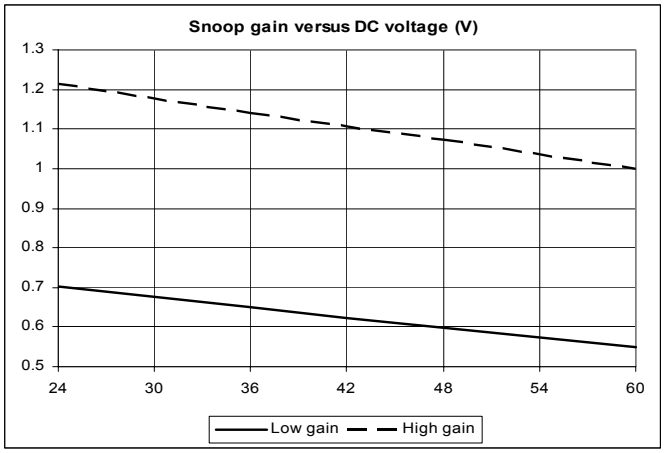


Figure 9: Snoop gain versus line DC voltage

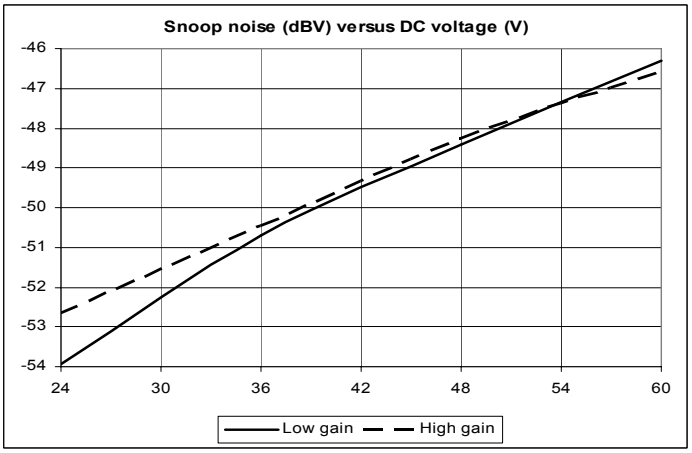


Figure 10: Snoop noise versus line DC voltage

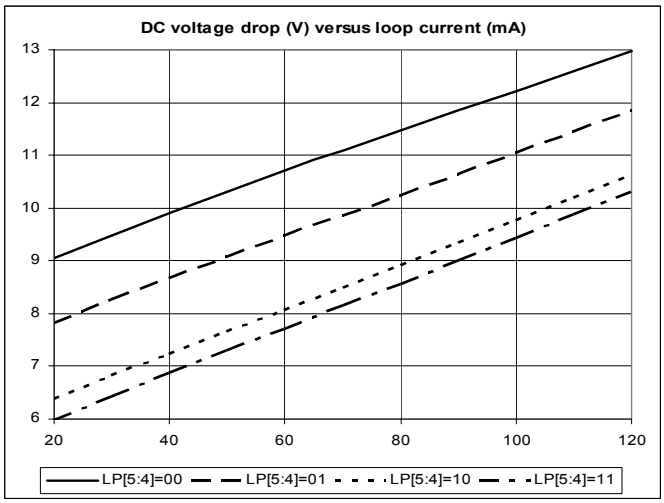


Figure 11: DC voltage versus current, no regulation

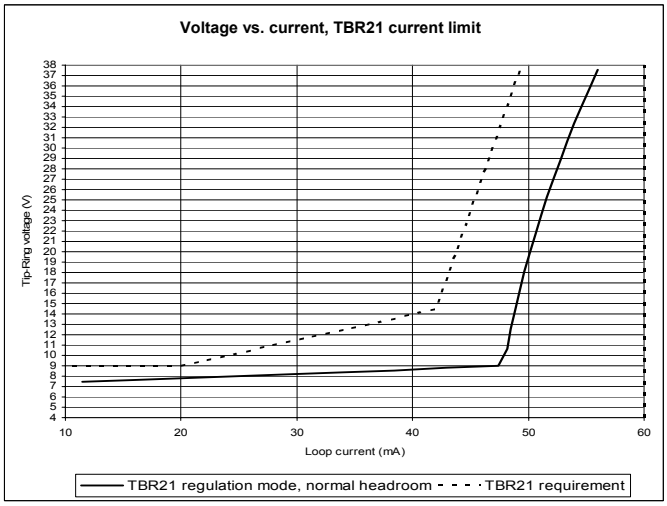


Figure 12: DC voltage versus current, TBR21 regulation

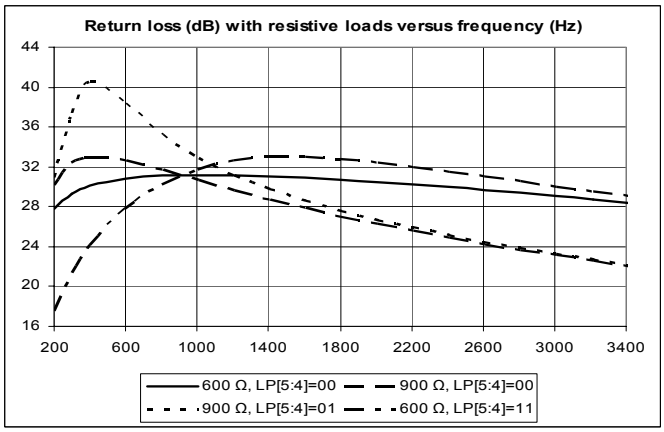


Figure 13: Return loss for resistive modes

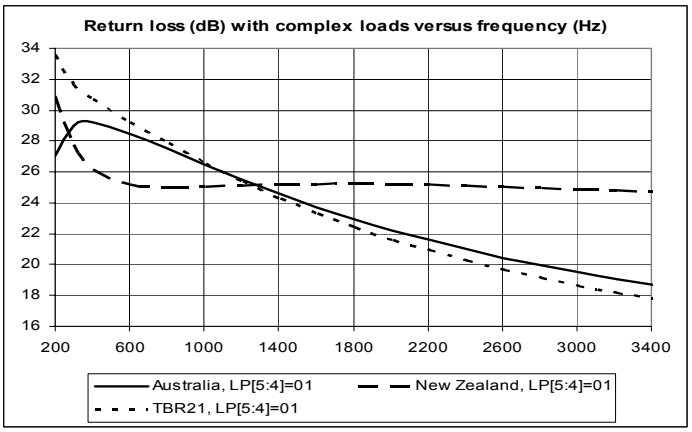


Figure 14: Return loss for complex modes

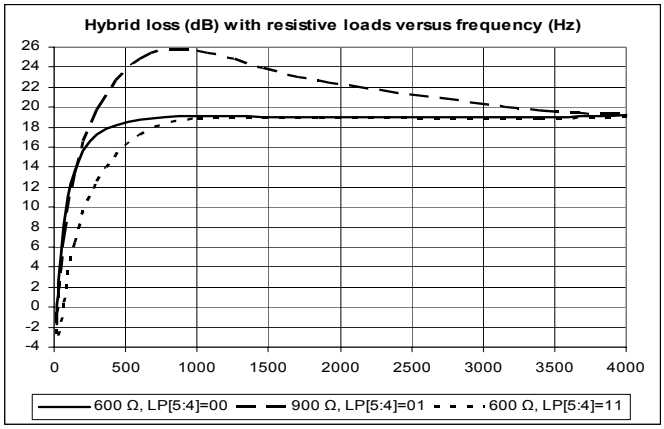


Figure 15: Trans-hybrid loss for resistive modes

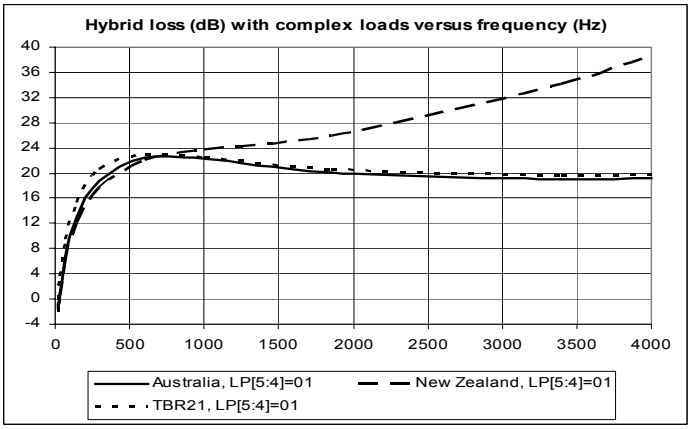


Figure 16: Trans-hybrid loss for complex modes

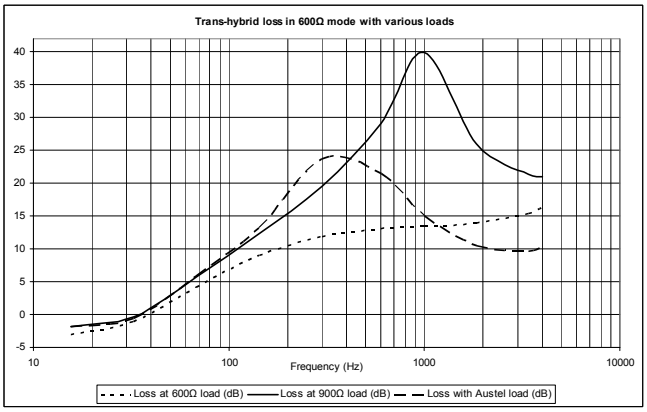


Figure 17: Trans-hybrid loss in 600Ω mode with various loads

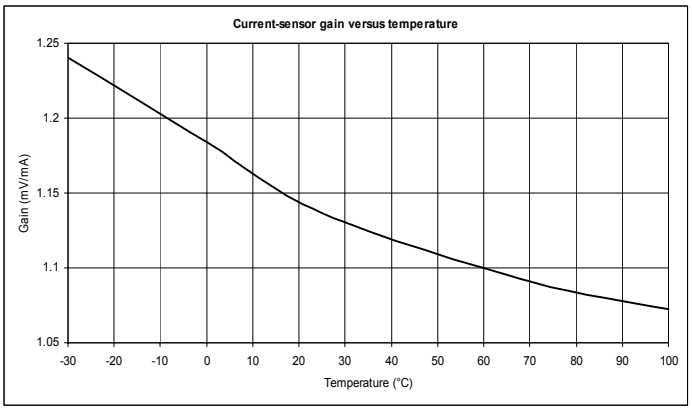


Figure 18: Current-sensor gain versus temperature s

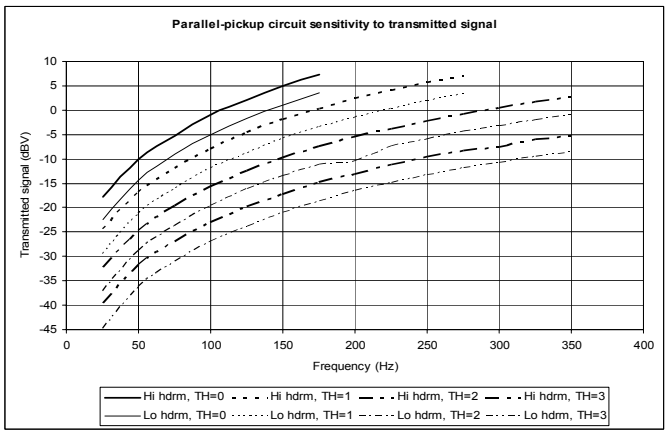


Figure 19: Parallel-pickup sensitivity to transmitted signals

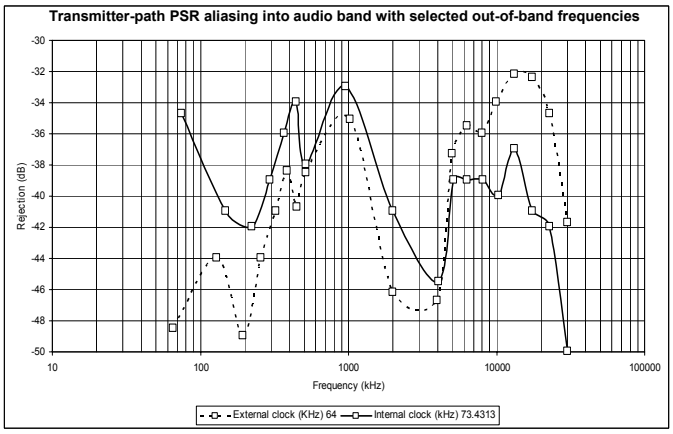


Figure 20: Transmitter-path PSR aliasing into audio band with selected out-of-band frequencies

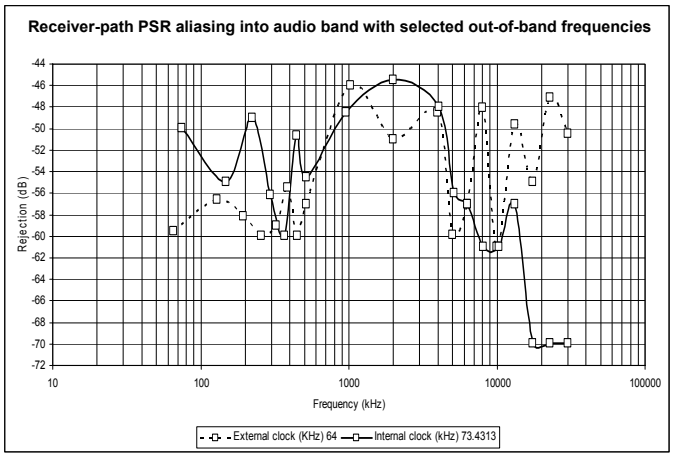


Figure 21: Receiver-path PSR aliasing into audio band with selected out-of-band frequencies

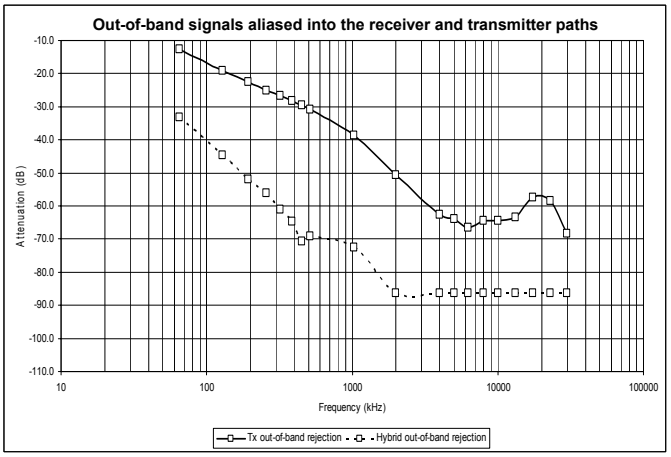


Figure 22: Aliasing into audio band (signals at selected out-of-band frequencies injected into Tx pin

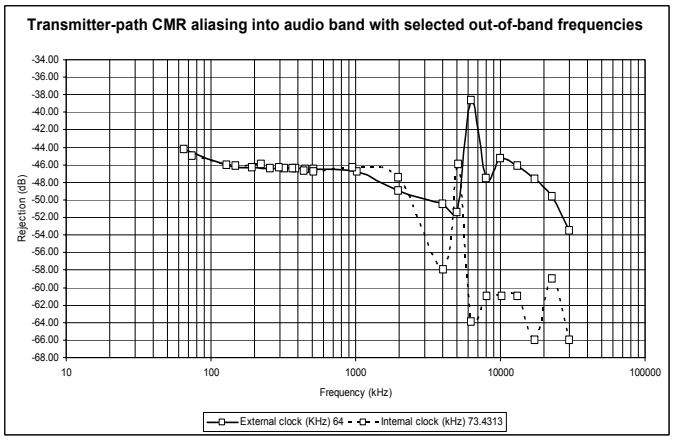


Figure 23: Transmitter-path CMR aliasing into audio band with selected out-of-band frequencies

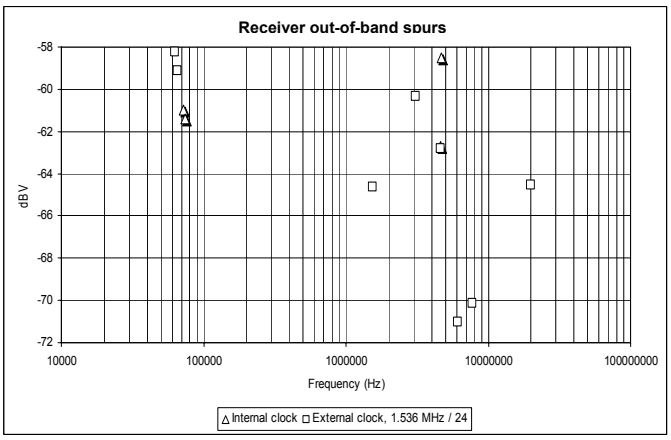


Figure 24: Receiver out-of-band spurs

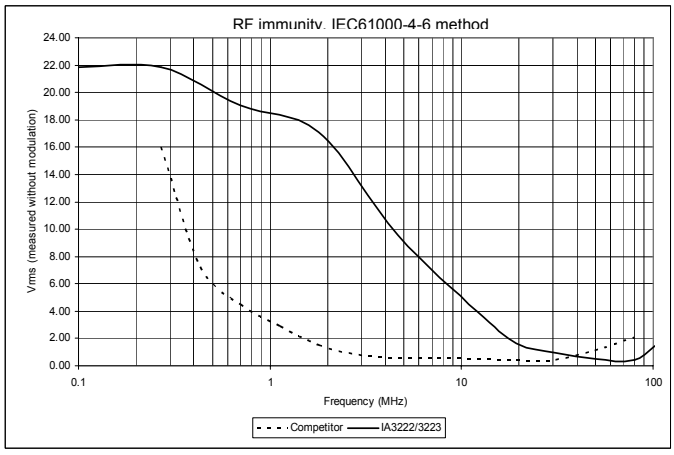


Figure 21: RF immunity, IEC61000-4-6 method

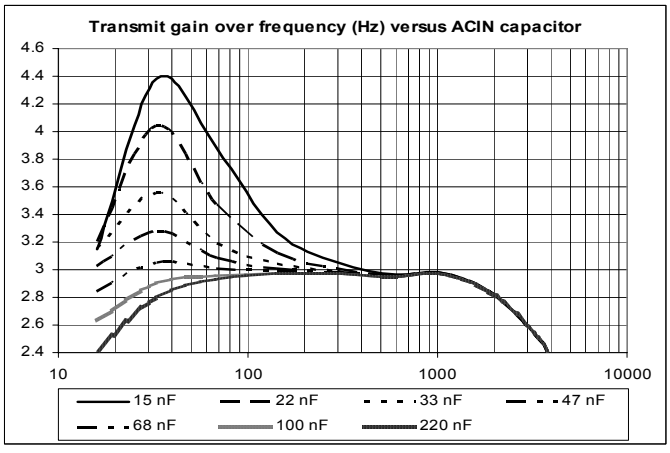


Figure 22: Transmit gain versus ACIN capacitor

REGISTERS

Register Map

A2	A1	A0	Register	D3	D2	D1	D0
0	0	0	Control	OFH	LSR	SGAIN	PWD
0	0	1	Line Side programming MSB	LP5	LP4	LP3	LP2
0	1	0	Line Side programming LSB	LP1	LP0	Reserved	REVID
0	1	1	Thresholds	LTH1	LTH0	RTH1	RTH0
1	0	0	Line status (read only)	RNG/PPU	LIU/LD	LACT	LP
1	0	1	Dividers	Reserved	F2	F1	F0
1	1	X	Reserved	Reserved	Reserved	Reserved	Reserved

Note: REVID is a read-only bit, hardwired to zero.

Control Register

Control bit	Definition	Function when low	Function when high	Reset state
OFH	Off-hook command	On hook	Off hook, ORed with OfHk pin	Low
LSR	Line Status Ring	Line-Status pin reflects the state of the LACT status bit (inverted).	Line-Status pin reflects the state of the RNG/PPU status bit (inverted).	High
SGAIN	Select gain	Low-gain Caller ID Normal transmit gain	High-gain Caller ID Additional 6 dB of transmitter gain	Low
PWD	Power down	Normal operation	Device powered down	Low

Note: Refer to the section on line monitoring for a description of the Line-Status pin.

Line-Side Programming Registers

LP5	LP4	Setting
0	0	High transmit voltage headroom and DC voltage drop (reset state)
0	1	Normal transmit voltage headroom and DC voltage drop
1	0	Low transmit voltage headroom and DC voltage drop (Note)
1	1	Lowest transmit voltage headroom and DC voltage drop (Note)

Note: This mode is not allowed in 600 Ω + 1µF or 900 Ω + 1µF impedance mode.

LP3	LP2	LP0	Setting	IA3222A	IA3222B	Cx required? (IA3222B only)	Cx1 required? (IA3222B only)
0	0	0	600 Ω or 600 Ω + 2.16 µF	Yes	Yes		
0	0	1	600 Ω + 1 µF (Note)		Yes		Yes
0	1	0	900 Ω		Yes		
0	1	1	900 Ω + 1 µF (Note)		Yes		Yes
1	0	0	ES 203 021, Australia or China complex impedance		Yes	Yes	
1	0	1	New Zealand complex impedance		Yes	Yes	Yes
1	1	0	TBR21 complex impedance with current limit		Yes	Yes	
1	1	1	Reserved				

Note: This mode is not allowed with low or lowest transmit voltage headroom.

LP1 Setting: 0, current sensor enabled; 1, current sensor disabled (recommended when current sensor is not required)

The Line Side is programmed when any of the following conditions is fulfilled: (1) after going from on-hook to off-hook; (2) when the Line Side LSB programming register is updated by the user or (3) after recovering from a loop-current interruption (line drop).

Threshold Register

LTH1	LTH0	Line-in-Use Threshold (VDC)	Parallel-Pickup Threshold
0	0	22.5 ±7.5 V (reset state)	0: least sensitive (reset state)
0	1	30 ±10V	1
1	0	15 ±5V	2
1	1	Line-disconnect detection (~2.5 V)	3: most sensitive

Note: The parallel-pickup threshold must be selected based on line usage and history. Depending on the application, selecting too sensitive a threshold may falsely detect a parallel pickup in the presence of large signals. Setting 0 or 1 is recommended for voice applications. Modem applications, where transmitted levels and frequency envelopes are well controlled, may benefit from using a more sensitive setting. Refer to Figure 6, which indicates the sensitivity of the detection circuit for signals of different frequencies for various settings. Note that the "high" headroom setting, (because of the reduced receiver gain), reduces the sensitivity of the parallel-pickup function by 3 dB. Each setting is approximately twice as sensitive as the previous setting.

RTH1	RTH0	No-Detection Ring Threshold (Vrms)	Ring Threshold (Vrms)
0	0	10 (reset state)	20 (reset state)
0	1	12.5	25
1	0	15	30
1	1	20	40

Line Status Register (Read Only)

Note: Writing any value to this register will reset all registers to their default values.

Mnemonic	Definition	Applicability	Status When Bit is Low	Status When Bit is High
RNG [Note 1]	Ring signal	On hook	Voltage below ring threshold	Voltage above ring threshold
PPU [Note 1]	Parallel pickup	Off hook	No loop-current drop	Loop-current drop
LIU [Note 1]	Line In Use	On hook	Voltage above LIU threshold	Voltage below LIU threshold
LD [Note 1]	Line Drop	Off hook	Line active	Line disconnected or line fault
LACT [Note 2]	Line activity	On hook	No change in line-in-use status	Change in line-in-use status
		Off hook	No parallel-pickup event	Parallel-pickup event
LP [Note 1]	Line polarity	On hook and off hook	Line reversed	Line direct

Notes:

1. This bit is multiplexed to a digital output pin of the IA3223A.
2. In the on-hook state, LACT will become high if the line voltage change is at least 10 to 20V in either direction.

Divider Register

F2	F1	F0	Clock Mode	Minimum Input Frequency (MHz)	Maximum Input Frequency (MHz)
0	0	0	Internal (reset state)	0.0672 (internal)	0.0828 (internal)
0	0	1	External divided by 24	1.38	2.0
0	1	0	External divided by 32	1.84	2.667
0	1	1	External divided by 48	2.76	4.0
1	0	0	External divided by 64	3.68	5.333
1	0	1	External divided by 96	5.52	8.0
1	1	0	External divided by 128	7.37	10.667
1	1	1	External divided by 1	0.0576	0.08333

Notes:

1. Table represents clock frequencies typically used for PCM interface devices.
2. An external clock can be used to synchronize an external codec with the DAA in order to avoid aliasing.

APPLICATIONS

Application Schematic

IA3222B for worldwide telecom compliance

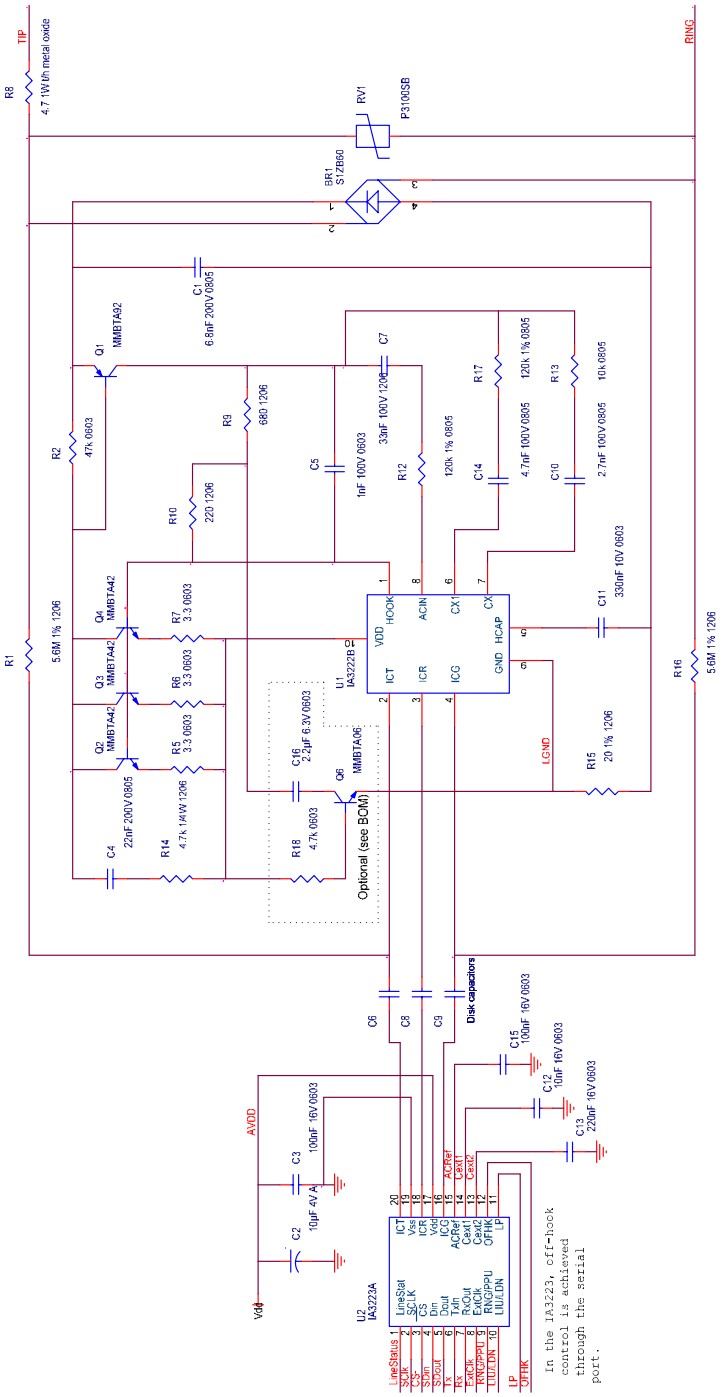


Figure 23: Application schematic

Bill of Materials

(All resistors are ±5% and capacitors ±20% tolerance unless indicated otherwise.)

Quantity	Reference	Part
1	BR1	S1ZB60
1	C1	6.8nF 200V 0805
1	C2	10µF 4V
2	C3, C15	100nF 16V 0603
1	C4	22nF 200V 0805
1	C5	1nF 100V 0603
3	C6, C8, C9	IsoBridge™ capacitors, drawn on PCB (Contact IAI for details.)
1	C7	33nF 100V 1206 (See note 1.)
1	C11	330nF 10V 0603 (See note 1.)
1	C12	10nF 16V 0603
1	C13	220nF 16V 0603
1	Q1	MMBTA92
3	Q2, Q3, Q4	MMBTA42 (See notes 2 and 3.)
1	RV1	P3100SB
2	R1, R16	5.6M 1% 1206
1	R2	47k 0603
3	R5, R6, R7	3.3 0603 (See notes 2 and 3.)
1	R9	680 1206
1	R10	220 1206
1	R12	120k 1% 0805
1	R14	4.7k 1206
1	R15	20 1% 1206
2	U1, U2	IA3222B
Option	C16	2.2µF 6.3V 0603 (only if more signal headroom is needed at the low or lowest headroom setting)
Option	Q6	MMBTA06 (only if more signal headroom is needed at the low or lowest headroom setting)
Option	R18	4.7k 0603 (only if more signal headroom is needed at the low or lowest headroom setting)
Option	R8	4.7 through-hole metal-oxide or other fusible resistor (only for UL 60950 or equivalent requirement)
Option	C10	2.7nF 100V 0805 (Use only if Cx is required. See note 4.)
Option	R13	10k 0805 (Use only if Cx is required. See note 4.)
Option	C14	4.7nF 100V 0805 (Use only if Cx1 is required. See note 4.)
Option	R17	120k 1% 0805 (Use only if Cx1 is required. See note 4.)

Note 1: For optimal audio performance, C7 and C11 should have a 250V rating and be of 1206 size. This is especially important for applications where the PCB is less than the standard 0.062" thickness, because ceramic capacitors are slightly piezoelectric and therefore sensitive to mechanical vibrations (microphonics). This effect is less pronounced with components of larger size and higher voltage rating.

Note 2: If the loop current is never more than 60 mA, Q4 and R7 may be omitted and R5 and R6 may be 2.2 Ohms.

Note 3: Do not replace Q2, Q3, Q4, R5, R6 and R7 with a single transistor of PZTA42 type. Power transistors with a higher gain-bandwidth product may be used, but they often are not cost effective. Refer to the component discussion for more details.

Note 4: C10 and C14 need to be NPO if V.90 modem performance is required. Otherwise, it is more cost effective to use X7R ceramic capacitors.

Application Schematic (Legacy TBR21 Current-Limit Support)

TBR21 current limit is no longer in force in Europe but may still be required for certain countries, e.g. Algeria, Bahrain, Croatia, Estonia, Ghana, Ivory Coast, Lebanon, Morocco and Turkey. This application is suitable for all other countries as well.

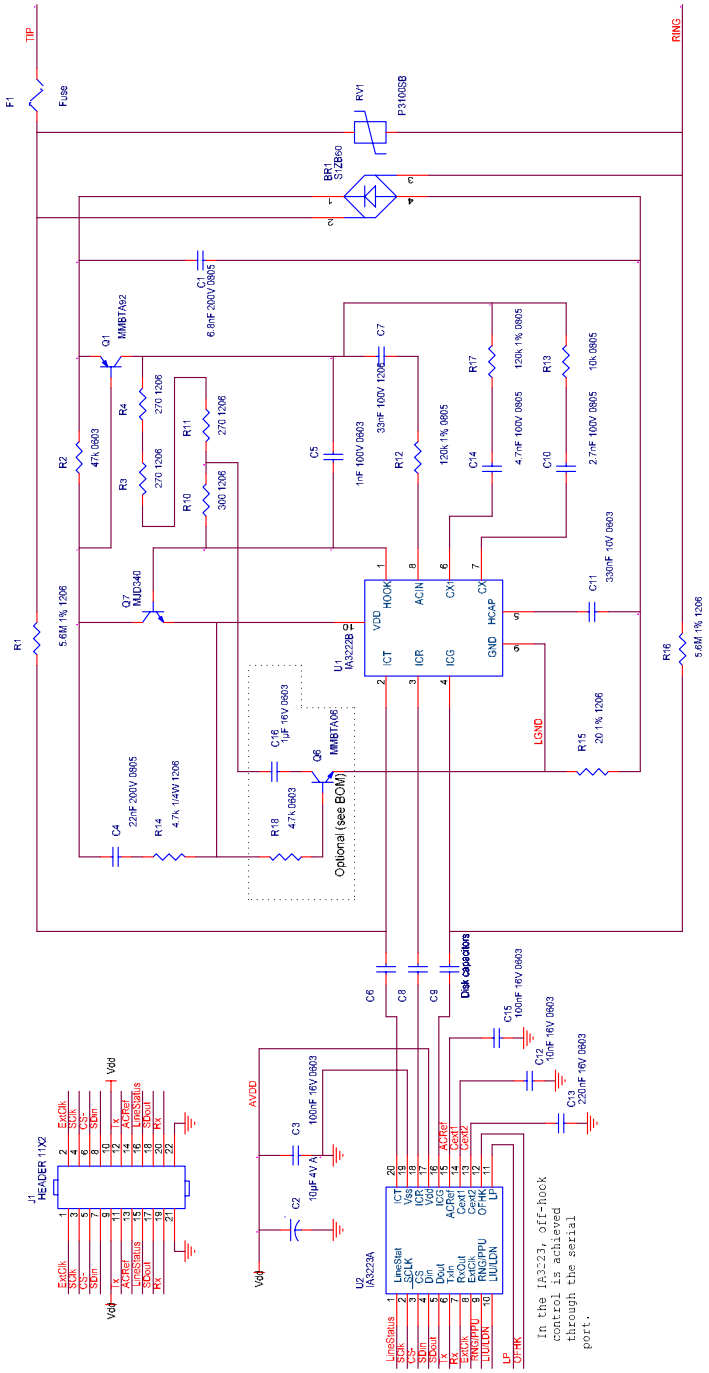


Figure 24: Application schematic for legacy TBR21 current-limit support

Bill of Materials (Legacy TBR21 Current-Limit Support)

(All resistors are ±5% and capacitors ±20% tolerance unless indicated otherwise.)

Quantity	Reference	Part
1	BR1	S1ZB60
1	C1	6.8nF 200V 0805
1	C2	10µF 4V
2	C3, C15	100nF 16V 0603
1	C4	22nF 200V 0805
1	C5	1nF 100V 0603
3	C6, C8, C9	IsoBridge™ capacitors, drawn on PCB (Contact IAI for details.)
1	C7	33nF 100V 1206 (See note 1.)
1	C11	330nF 10V 0603 (See note 1.)
1	C12	10nF 16V 0603
1	C13	220nF 16V 0603
1	Q1	MMBTA92
1	Q6	MJD340
1	RV1	P3100SB
2	R1, R16	5.6M 1% 1206
1	R2	47k 0603
3	R3, R4, R11	270 1206
1	R10	300 1206
1	R12	120k 1% 0805
1	R14	4.7k 1206
1	R15	20 1% 1206
2	U1, U2	IA3222B
Option	C16	1µF 16V 0603 (only if more signal headroom is needed at the low or lowest headroom setting)
Option	Q6	MMBTA06 (only if more signal headroom is needed at the low or lowest headroom setting)
Option	R18	4.7k 0603 (only if more signal headroom is needed at the low or lowest headroom setting)
Option	F1	Fuse (only for UL 60950 or equivalent requirement)
Option	C10	2.7nF 100V 0805 (Use only if Cx is required. See note 2.)
Option	R13	10k 0805 (Use only if Cx is required. See note 2.)
Option	C14	4.7nF 100V 0805 (Use only if Cx1 is required. See note 2.)
Option	R17	120k 1% 0805 (Use only if Cx1 is required. See note 2.)

Note 1: For optimal audio performance, C7 and C11 should have a 250V rating and be of 1206 size. This is especially important for applications where the PCB is less than the standard 0.062" thickness, because ceramic capacitors are slightly piezoelectric and therefore sensitive to mechanical vibrations (microphonics). This effect is less pronounced with components of larger size and higher voltage rating.

Note 2: C10 and C14 need to be NPO if V.90 modem performance is required. Otherwise, it is more cost effective to use X7R ceramic capacitors.

Component Discussion

The application schematic (Figure 23) is intended as a high-density surface-mount solution. When using through-hole components, some changes may be possible in the design. Please contact IAI support for these issues.

The main hook switch is composed of three parallel NPN transistors (Q2–Q4) and three emitter ballasting resistors (R5–R7). This structure is necessary when using low cost, generic 300 V telephone application transistors in order to keep these transistors out of their quasi-saturation region at high loop currents.

With the use of qualified transistors, it is possible to reduce the transistor count on the NPN hook switch but may not be cost effective or reduce board area. Although 300V rated telephone hook-switch application transistors only cost pennies, they work best as switches and tend to behave poorly when operated in their linear region at currents above 20 mA, with only a few volts drop from collector to emitter. This is due to quasi-saturation effects that reduce their frequency response to only a few MHz. Even the SPICE models for these devices designed over 30 years ago are often inadequate in these linear operating regions. If too few of these transistors are used in the hook circuit, stability issues at higher loop currents may occur. As an alternative, more recently designed high-voltage NPN transistors in larger packages (for power dissipation) can be used to construct either a double or single hook switch but may easily cost more than the three-parallel NPN solution. Without extensive characterization, IAI does not recommend alternative hook-switch transistor solutions except the one provided for legacy TBR21 support (see below).

High-density ceramic capacitors can cause both microphonic and distortion problems due to piezoelectric effects (mechanical strain) and voltage coefficients (changes in capacitance with voltage). In general, the higher a ceramic's dielectric constant, the greater its voltage-dependency and piezoelectric effects. The lower the voltage rating on a ceramic capacitor, then the higher the voltage gradient across the dielectric. This means that a capacitor of lower voltage rating and same dielectric material will have worse voltage distortion and electromechanical effects.

IAI has identified which capacitors are most likely to be critical with respect to these issues on the application schematic. It is possible to use different dielectric material for these capacitors if the devices are physically larger and the customer can evaluate the board for possible increased distortion or electro mechanical effects in the end product.

Legacy TBR21 support is possible but not recommended since so few countries require it and the standard has been superseded. Current limiting is now obsolescent if not obsolete. In order to meet TBR21 current limit, a DAA needs to dissipate 2 W safely. In the IA3222/3223 application, about half of this power is dissipated in R3, R4, R10 and R11 and the other half in the NPN transistor.

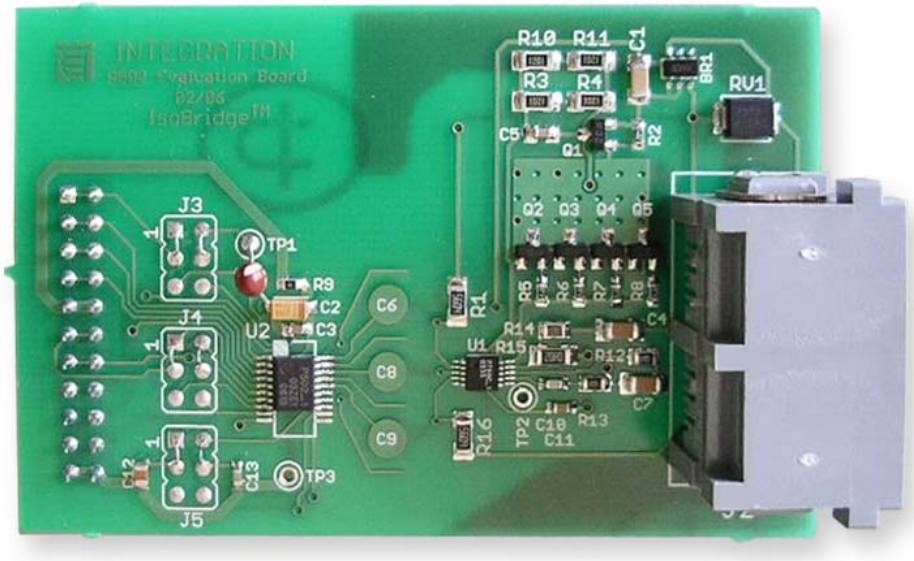


Figure 25: IA3222/3223 evaluation board

Sample Layout

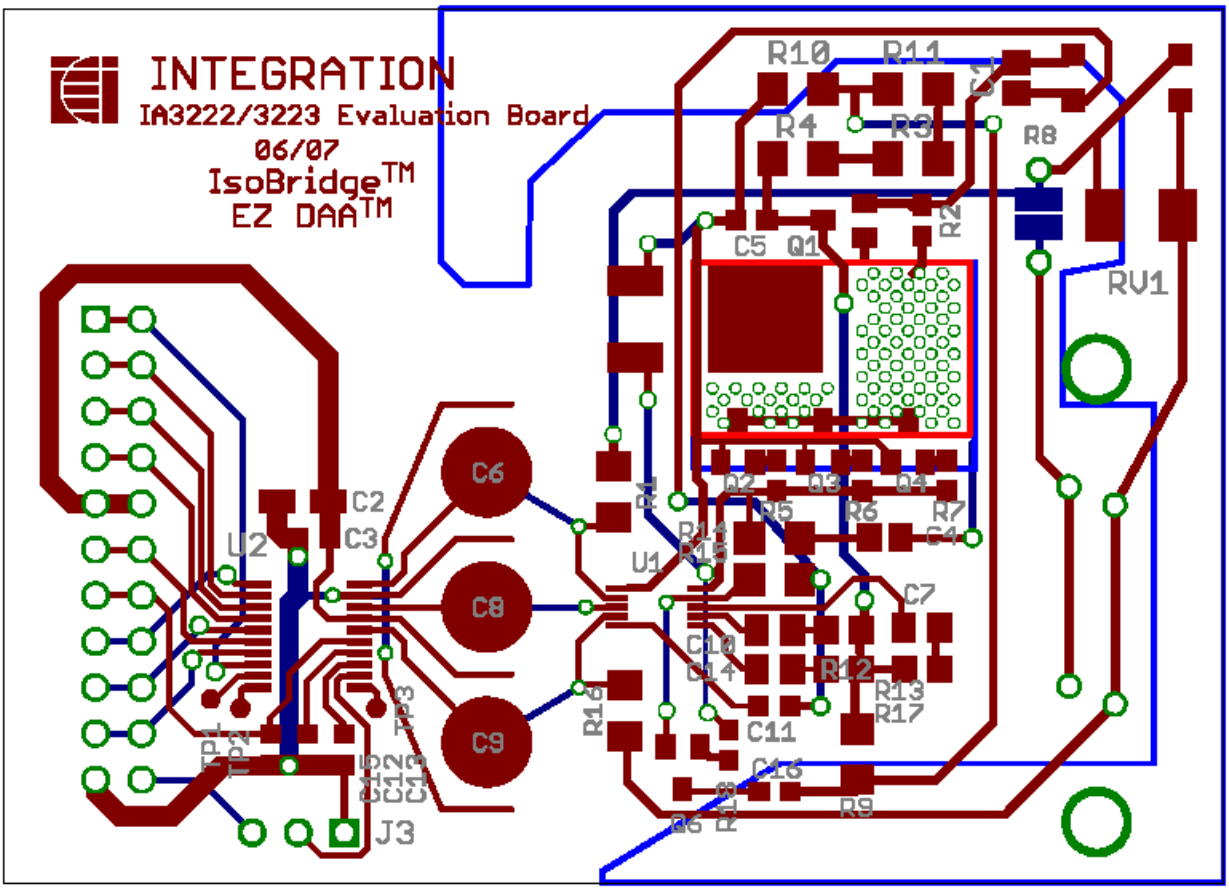


Figure 26: IA3222/3223 evaluation board layout

Layout Guidelines

- Minimize trace lengths between U1, R1 and R15.
- Disc capacitors and their connecting traces should be drawn exactly as shown, with 4.95mm (195 mils) diameters, 2.5mm (98.5 mils) spacing and 10-mil traces in between on the system side only. All dimensions must match. This assumes a standard board thickness (0.062") and FR-4 material. Contact IAI for other board thicknesses or materials.
- Carefully observe the required creepage distance (surface distance over isolation) for surge rating. There must be at least 2.5mm (98.5 mils) between any line-side conductive trace and any system-side conductive trace, including the mounting holes if the are electrically connected. Because of PCB manufacturing tolerances, the minimum drawn distances should be about 2% larger, or 2.55mm (100.5 mils). It is a good practice to designate a "preferred arc path" between the Tip and Ring lines and the chassis, e.g. at the RJ-11 connector, by drawing those at the minimum required distance, while all other spacings between Line Side and System Side are drawn lightly larger, e.g. 2.8mm (110 mils).
- Put no metal markings in the area of the disk capacitors. This must be watched closely, since PCB manufacturers routinely add markings wherever they find it convenient, possibly shortening the creepage distance.
- For optimal audio performance, minimize trace lengths between the System Side and its supply-decoupling capacitors.
- Q2, Q3 and Q4 should be laid out with a lot of extra copper on both sides of the board with thermal vias in order to facilitate heat dissipation.

Interfacing the IA3223

The simplified block diagram below shows single ended interface to A/D and D/A. The analog interface consists of 3 pins:

- **TX** – audio input
- **RX** – audio output
- **ACREF** – AC voltage reference

There are two ways to interface to A/D and D/A:

DC coupling

All three pins TX, RX and ACREF are connected to the codec directly. The ACREF pin has a weak internal buffer (refer to DC characteristics table), which can be overdriven easily with an external reference. The external reference voltage must be in the 1.2V to 1.8V range. Connecting the codec's AC reference to the ACREF pin will insure good common mode rejection.

One of the advantages of DC coupling is an alternative way for the host processor to detect parallel pick-up (PPU). PPU may be detected using LINESTAT pin, as described in the next section. The alternative way is to monitor the DC offset at the RX pin. (Line-Side programming bit LP1 must be set to zero.) The DC loop current is added to the RX signal as a DC offset with a gain of about 1 mV/mA. Applying a digital low-pass filter to the RX channel audio enables the detection of a drop in the DC loop current, thus indicating a PPU event.

AC coupling

All three pins TX, RX and ACREF may also be connected to codec using coupling capacitors. For the ACREF pin, a capacitor of at least 100nF is recommended. All coupling capacitors should be selected so that they will not cause any significant attenuation at low frequencies, taking input resistances into account. The TX pin is internally biased at 1.5V.

Please contact Silicon Labs for additional assistance with interfacing the IA3223.

Interfacing Examples

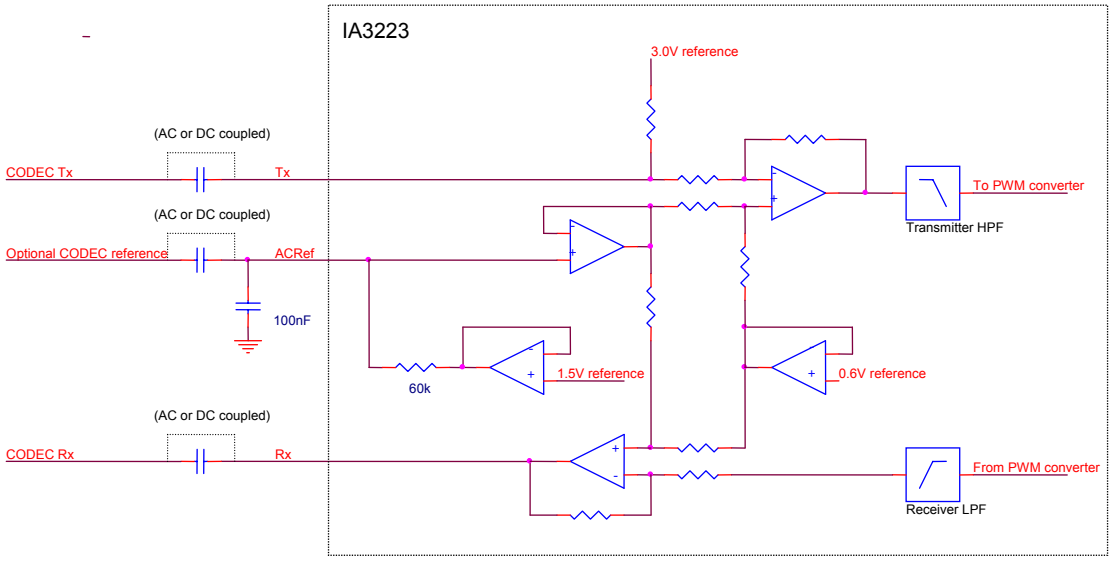


Figure 27: Single-ended interface

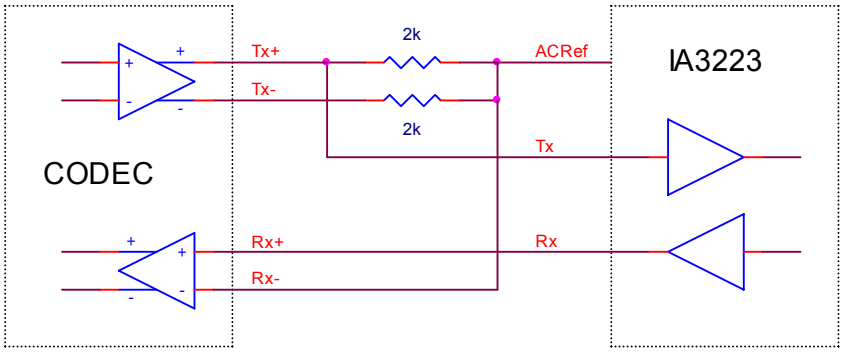


Figure 28: Differential interface — without reference

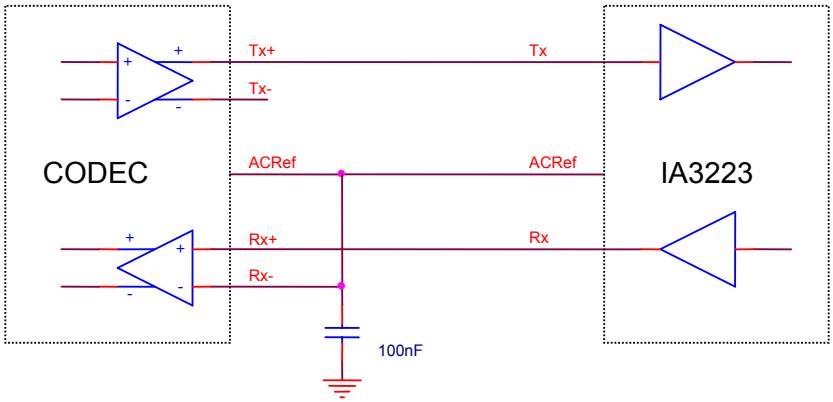


Figure 29: Differential interface — with reference

LINE MONITORING

Theory of Operation—On-Hook Line Status

The IA3222/3223 chipset was designed to provide maximum information about the telephone line—both AC and DC—to allow intelligent line management, and to allow automatic telephone devices to share the line with human-controlled applications gracefully. Automatic DAA applications may be found in set-top boxes, alarm systems, fax machines, meter readers, remote-diagnostic modems, answering machines, VoIP boxes, etc. A key feature of the IA3223 is the LineStat pin, which can be programmed to generate an interrupt if the line status changes either while in the on-hook state or in the off-hook state. This reduces the need for continuous polling of the line-status bits.

In the on-hook state, the IA3222 Line Side chip converts the line voltage to a frequency at the rate of 2 kHz per Volt. The V-to-f's operating range is from ±3V to over ±150V. This frequency is sent as pulses across the capacitor isolation barrier. The pulse duty cycle contains line-polarity information. The V-to-f converter's frequency is sufficient to allow the IA3223 System Side to decode all DC line voltage, ring signals, line reversals and audio information (Caller ID, DTMF, and other tone monitoring). While monitoring the line in the on-hook state, the Line Side loads the line with no less than 5 MΩ DC resistance. This allows continuous monitoring while exceeding regulatory minimum idle-line resistance requirements.

The IA3223 System Side chip receives the frequency-encoded voltage information and converts it back to continuous representation of the line voltage. The voltage difference between the ACRef pin and the CExt2 pin is about 1/200th of the line voltage. Since the DC source resistance of CExt2 is about 75 kΩ, any measurement system resistance should exceed 10 MΩ to prevent excessive loading.

For the on-hook snoop function, CExt1 is part of a gyrator circuit that separates the large DC line voltage from the low-level AC voltage, so that the line audio signal may be amplified without excessive offset. CExt1 sets the low-frequency corner on this gyrator circuit inversely proportional to its value. With 10 nF, the -3 dB corner is around 240 Hz and the slope is 6 dB per octave. The upper-frequency corner is around 4 kHz. It is set by internal RC values, and is therefore not adjustable by the user. The upper-frequency roll-off exceeds 18 dB per octave.

In the on-hook state, CExt2 filters the line voltage analog with a time constant of CExt2 times 75 kΩ, for separating the AC ring signal from the DC line voltage. With a CExt2 of 220 nF, the corner frequency is about 10 Hz. The ring-detection circuit compares the voltage on CExt2 with an internal unfiltered signal. If it exceeds one of the four programmable thresholds in one direction, a ring-detection condition occurs. This produces a standard half-wave ring-detection signal that works similarly to a standard opto-isolator ring-detection circuit.

In addition to ring detection, the other on-hook functions are a line-polarity (LP) detector, a line-in-use detector (LIU) and a line-activity (LACT) detector. The LIU detector measures if the line voltage exceeds one of four programmed voltage levels. The LACT detector output is activated if the line voltage changes by more than 10 to 20V, thus acting like a sensitive full-wave ring detector. All of these signals can be read from IA3223 registers. Depending on the setting of the LSR bit, either the ring-detection signal or the LACT signal can be output to the LineStat (line status) pin.

Ringing

The IAI 3223 supports conventional ring-detection algorithms that produce an on-off digital output when the AC signal exceeds a preset threshold. The period between cycles is measured by the system firmware to within 1-2ms to allow qualification of ring cycles in order to differentiate them from other line signals: notably on-/off-hook transients, dial pulses and test signals sent by the telephone company. The ring-detection state is presented on read-only register RNG bit and may optionally be multiplexed to the LineStat pin. The width of the ring-detection pulse is always at least 20 % of the ring period for sine-wave ring signals.

Many regulatory ring requirements have disappeared in the last fifteen years and the usage of pulse dialing has also decreased. In more ancient telephone history, when telephone companies were monopolies, 10 V_{RMS} signals were sent down telephone lines in order to determine how many ringer loads were present. Although this probably no longer occurs, conventional wisdom is that ring detectors should not trip below 10 V_{RMS}. Many country-specific regulations and EIA/TIA recommendations support this requirement to this day.

The most common spurious ring detection is due to pulse dialing. In Japan, 20 pulses per second used to be common. The simple way to prevent spurious ring detection from dial pulses is to set a sufficiently high ring-detection threshold. In countries that have strong ring signals, setting one of the upper two thresholds (22.5 or 30 V_{RMS}) will prevent ring detection of most of the dial pulses. The first pulse may still be detected, because the initial dial pulse or off hook transient may present a large signal to the ring-detection circuit. Subsequent dial pulses will fall below the ring threshold as the DC-averaging circuit centers the AC waveform. This problem can be seen with all conventional ring detectors. This is why ring-detection algorithms always need to qualify at least two ring cycles by ensuring they fall within the time limits that correspond to the possible ring frequency.

In some countries (e.g., the UK and Australia), low ring thresholds are desired. Rather than setting parameters of ring threshold, period, and number of valid cycles for each and every country, it is simpler to divide the whole world into a few separate ring qualification groups. Valid ring signals are between 15 and 68 Hz. Ring cadences are never more than 2 seconds on but may be as little as 0.2 seconds for distinctive ringing. If a 1ms period resolution is available, and assuming a tolerance of ±10 % ±1 ms, the valid period range is 12 to 74 ms. These period limits screen out 10 pps but not 20 pps pulse dialers. An example of two ring qualifier groups would thus be:

- Set lowest ring threshold (15 V_{RMS}), qualify ring period 12 to 74 ms, require at least two to three valid periods in a row (disqualify if any period falls outside this range). This works worldwide except for 20 pps pulse dialing.
- For strong ringer countries (e.g., North America and Japan), use the same criteria but set the ring threshold to 30 V_{RMS}.

Line reversal (LR), line in use (LIU), or line activity (LACT) may also be used for ring detection in limited circumstances. Line reversal is probably safe in high ringer-threshold countries and would reject 20 pps dial pulses effectively. In low ringer-threshold countries, it may not reliably detect weak ring signals since the ringer signal typically rides on top of the DC line voltage. If the ringer AC peaks are less than the line voltage, line reversal will not occur.

LACT and LIU will almost always be triggered on any ring signal but qualifying the ring frequency is a problem because both detectors may produce more than one pulse per ring period. Although LACT is a sensitive full-wave ring detector, full-wave ring detectors are less accurate with period because ring signals can be asymmetric either because of origination or because of loading. In addition, the LACT detector is not as precise as the ring detector. Its threshold may vary from 10 to 20V peak.

Another ring-detection scheme makes use of the snoop audio output available at the RxOut pin. If the -6 dB snoop gain is set (SGAIN bit set to zero) and if the CExt1 corner is placed correctly, the ring signal will be available in the snoop audio path with sufficient attenuation to avoid clipping. A CExt1 of 10 nF will work well for typical 20 Hz ring signals. If the ring signal is expected to be around 50 Hz, CExt1 should be reduced to 4.7 nF. This will increase the -3 dB high-pass corner of the snoop audio path to about 700 Hz, which is normally acceptable for Caller ID signals.

Line Reversal

On-hook line reversal (not to be confused with off-hook loop current reversal) occurs in some countries instead of the first ring cadence before the Caller ID message. Line reversal may also be used for other signaling. Typically, many DAAs with line-reversal detection capability can only detect the transient and not the actual line polarity, making it difficult to differentiate a line reversal from an off hook transient. The IA3223 has a true line-polarity detector. Line polarity is directly sensed in the IA3222 Line-Side chip and this information is sent across the isolation barrier to the IA3223 System-Side chip. Line polarity reversal may take up to 50 ms. Through this transition all three detectors Line In Use, Line Activity, and Ring may be triggered. A line reversal can be qualified by determining if the change in polarity is stable for 50 to 100 ms.

Line Activity

The LACT detector can be programmed to drive the LineStat interrupt pin. This avoids the need for continuous polling of either the LP (line polarity) or RNG (ring detection) bit. LACT detects 10 to 20V changes in either direction, also triggering on any ring, line reversal, or hook status change. When a LineStat interrupt occurs, the system would poll the RNG, LP, and LIU bits and apply qualification algorithms for about 100 ms or until line activity stops.

Line in Use and Line Disconnect

The LIU detector is a DC line-voltage threshold detector. One of four levels (~2.5, 15, 22.5, and 30V) can be selected. Unfortunately, line-in-use status is ambiguous for voltages between 12V and 19V. Central Office lines and short-range digital loop carrier systems always provide at least 21V of on-hook voltage. Some PBXs and VoIP boxes may supply less. Telephone devices will generally work with less than 12V at a loop current of 20-30mA. Users sometimes add in-line Zener devices (available at Radio Shack®) in series with answering machines in order to improve parallel-pickup disconnect performance. These in-line Zener devices increase the answering machine's off hook voltage by 6 to 8V, often pushing the total off-hook voltage above 15V. On short loops with 60mA capability, some telephone devices may drop over 12V when off hook. European telephone devices with CTR-21 current limiting may even exceed 32V when off hook on short lines, especially in France.

For most situations, the 15V LIU threshold setting should be the default. A simple technique to reduce ambiguity is to use both LIU and snoop audio detection. A more sophisticated method is to have the system learn normal on and off hook voltages by stepping through the LIU levels of 15, 22.5 and 30V while using the snoop circuit to monitor audio.

The 2.5V threshold setting is intended to differentiate a disconnected line (not plugged in) from a powered line without attempting to distinguish on hook from off hook. A disconnected line may create erratic 2.5V and line-reversal detection. This is because the Line Side has over 5 MΩ input resistance. Less than 100 nA of on-hook loop current can trigger the 2.5V threshold. This behavior is similar to putting a standard 10 MΩ input voltmeter on a long open line and seeing several Volts due to static or leakage. Generally, a valid line is present only if the voltage is stable above 3V and not reversing. If it is below 2V or reversing, the line should be considered disconnected. Off-hook loop-current reversal (if available on a trunk) occurs only after dialing to indicate far party answer (toll call).

The LineStat Pin as Interrupt (On Hook)

The LineStat pin is an active-low interrupt output. Because it has an open-drain output with a weak internal pull-up resistor, it can be wire-ORed with other interrupts in the system. When LineStat is active, the system must determine the cause of the interrupt based on history and the state of the DAA. The table below suggests criteria for qualifying the interrupt when the DAA is on hook:

LSR required setting	Possible Cause of Interrupt	Criterion
High	Ringing	Expected ring cadence both at LineStat pin and at RNG bit
Low	Line reversal	LP bit changed compared to before interrupt, stable for 100 ms
	Line in use	LIU bit high if previously low, stable for 100 ms
	Line no longer in use	LIU bit low if previously high, stable for 100 ms
	Line activity	No ring cadence or change in LP or LIU bits

Audio Snooping

The snoop circuit does not have the same audio performance as the off-hook receiver path, but it is adequate for Caller ID decoding and line monitoring. Snoop audio recovers from all high voltage line signals in less than 10 ms and is continuously present. Besides Caller ID, snooping can be used to monitor the line for call logging or used for voice/fax steering. If a fax calling tone or a specific DTMF sequence is detected, the DAA may be instructed to seize the line. Since DTMF signals normally have higher amplitude than Caller ID signals, a -6 dB gain setting exists for the snoop path (SGAIN set to zero), which allows monitoring of up to 4 VPP signals without clipping.

Theory of Operation— Off-Hook Line Status

In the off-hook state, the same gyrator circuit that is used for on-hook line-status monitoring is reconfigured to filter audio signals from the line-current change circuit (parallel-pickup detector), so that changes in loop current can be measured without spurious parallel-pickup signals from normal audio. Capacitor CExt2 with an internal 1.2 MΩ resistor forms large time constant that stores the average DC value of the received signal. This DC value is compared with short-term changes to detect loop current drops caused by a parallel phone on the line going off hook. Sensitivity to parallel pickup is also affected by the IA3222 Line-Side's holding and AC-input capacitor values. There are four levels of parallel-pickup sensitivity, programmed by register bits LTH0 and LTH1. Each setting is about twice as sensitive as the previous. When a parallel-pickup event occurs it causes a temporary active state both at the PPU (Parallel Pick Up) bit and at the LineStat pin.

Line Drop

Line drop or wink is a complete drop in loop current from the Central Office switch, usually indicating call disconnect or call waiting depending on the duration of the drop. Drops over 500 ms indicate disconnect while shorter drops indicate call waiting. Consequently, it is important to time the duration of line drops with at least 10 ms resolution. Line drop is detected by the IA3223 System Side and flagged as the LD (Line Drop) status bit when the IA3222 Line Side receives insufficient loop current to keep it operational (less than 10 mA).

Parallel Pickup

Generally, the primary reason for parallel-pickup detection is to allow automatic telephone devices (set-top box modems, fax machines, etc.) to drop the line if a parallel telephone device attempts to dial. When a parallel telephone device goes off hook, the loop current into the IA3222 Line Side decreases. The parallel-pickup circuit detects the low-frequency (less than 100Hz) transients associated with a parallel pickup or hang up. To prevent spurious detects due to large, low frequency audio signals, the parallel-pickup circuit attenuates audio-band signals. At the most sensitive setting, the parallel-pickup circuit will spuriously detect maximum amplitude voice and DTMF signals but not modem signals. Parallel pickup dI/dt may be very low either because the parallel phone has a high off hook voltage relative to Line Side IC or because the parallel phone holding circuit (electronic inductor) may turn on slowly. The parallel-pickup circuit must therefore be very sensitive.

In a modem or fax application, lower parallel-pickup sensitivity can be set when dialing DTMF tones to prevent a spurious detection. A higher sensitivity can then be set after dialing. Typically, a -10 dBm modem signal transmitted from the DAA will not trigger the parallel-pickup detector on its most sensitive setting. One method for setting the levels is to raise the sensitivity until spurious detects occur and then reducing the sensitivity by one step. Each step has about a 6dB difference in sensitivity.

Because the transmit-to-receive trans-hybrid return loss is poor at frequencies below 100 Hz, it is important that there be no low-frequency transients in the transmitted audio signal, so as to prevent spurious parallel-pickup detections. Modem software can create low-frequency settling transients when switching modes, typically during training or DTMF dialing. These may cause spurious parallel-pickup detections. If adjusting the modem software is not possible, another solution is to put a low-frequency blocking capacitor in the transmit path.

The LineStat Pin as Interrupt (Off Hook)

In the off-hook state, the LineStat pin behaves in a way similar to the on-hook state. The table below suggests criteria for qualifying the interrupt when the DAA is off hook:

LSR required setting	Possible Cause of Interrupt	Criterion
High	Line drop	LD bit high
	Loop-current reversal	LP bit changed compared to before interrupt
	Parallel pickup	PPU bit high

Measuring Loop-Current Changes through the Received Audio signal

The Line Side senses line-current information and encodes it for the System Side as a DC offset superimposed onto the received audio data. Since modem DSP algorithms routinely remove low-frequency components from the incoming data stream, DC offset is not a problem, but it needs to be taken into account in headroom calculations.

The current sensor has considerable DC offset, which needs to be calibrated to obtain good current-sensor performance. This is achieved by adding a DC component to the transmitted data proportional to the received DC offset using the following algorithm:

- Disable the current sensor by setting bit LP1 in the Line-Side LSB programming register. This cancels the DC component due to the loop current itself and leaves the current sensor's offset component as DC offset in the received data stream.
- Add a small amount (20 to 50mV) of DC offset to the outgoing data and note the amount of change in DC offset in the incoming data. The ratio of incoming to outgoing DC offset changes is the DC-offset correction factor, for which the sign must be retained.
- Add a DC offset to all transmitted data equal to the received DC offset divided by the DC-offset correction factor, based on the desired DC reference for the received signal. This is normally the same voltage as that of the ACREF pin.
- Enable the current sensor. The loop current can now be read as incoming-data DC offset from the DC reference voltage. The sensitivity of the current sensor is approximately 1.25 mV of DC offset for every 1 mA of loop current. Note that both the DC-offset correction factor and the gain change with the Line-Side termination impedance setting.

SURGES, ISOLATION AND EMC

Among the three regulatory domains that DAAs must comply with (telecom, safety and EMC), safety and EMC tend to be highly intertwined. Designing for regulatory approval can sometimes compromise field reliability of DAAs. Historically, the dominant cause for field failures of modems or other DAA-based telephone products has been electrical overstress from the telephone line, typically due to lightning, ESD, or incompatibility with digital PBX lines. The most common failures are both metallic (differential) and longitudinal (common mode). Metallic failures are evidenced by damage to components on the line side while longitudinal isolation failures usually damage the drivers or receivers on either side of the isolation barrier. Overdesigning for surge immunity is not uncommon with DAAs. This can add as much as a dollar in costly surge components compared to what is necessary to pass required regulatory testing or field stresses, which are often poorly understood. Even minimal surge and regulatory isolation components may be the most expensive non-IC components in the DAA Bill of Materials. Moreover, contrary to expectation, more robust surge components may actually make the DAA less robust overall.

For regulatory, functional and safety reasons, DAAs provide isolation and protection against excessive voltages and currents. The telephone line system provides DC and AC common-mode ground at the current-source end of the line. At the user end or CPE (Customer Premise End), the telephone device must be insulated either inherently or using a DAA.

The classic example of inherent isolation is the standard telephone, which is not connected to the AC mains. But commonly, answering machines and cordless telephones also are completely insulated despite being powered by the mains. In these products, two-prong transformer wall supplies provide the safety isolation. Products that have a third prong safety ground on the power plug almost always use a DAA for the loop interface. If a product has a conductive chassis or has other electrical connections, it usually will need a DAA to interface to the telephone line. Examples in this group are alarm systems, set-top boxes, fax machines, remote meter readers, etc.

Functionally, longitudinal isolation at the CPE is the optimum solution for achieving very high common-mode noise rejection. Repetitive longitudinal transients on the telephone line twisted pair may exceed 10V peak and continuous AC may exceed 70 V_{RMS} (+40 dBm). Since the basic audible noise floor is around –75 dBm, this is over 110 dB of dynamic range. Only dielectric isolation provides both very large common-mode range without overload and excellent common-mode rejection.

As in medical instrumentation systems, dielectric isolation, besides providing high common-mode immunity, also provides safety isolation against electrical shock, overstress damage and fire. Generally, these latter issues are the concern of regulatory safety standards. In many markets, the telephone line interface must satisfy these requirements strictly.

Consequently, DAAs provide a unique challenge in consumer products, needing to meet industrial isolation and robustness but at consumer prices, unlike the industrial SLIC (Subscriber Line Interface Circuit) on the other end of the phone line. Traditionally, SLICs are part of the total cost of the local telephone line that may have a capital value of $1000 that is amortized over a forty-year life. For every industrial SLIC sold, there may be twenty consumer telephone devices sold.

Safety Isolation and Differential Surges

The sources of safety or damage causing electrical stress are lightning-induced transients, ESD (electrostatic discharge), AC power-line crosses, AC power line transients, and incompatibility with digital PBX phone power. Proper DAA design can eliminate these hazards.

Lightning-induced transients and ESD are very similar in behavior and the damage they cause. Generally, the best remedies for one work well for the other. Lightning transients come down the telephone line from outside while ESD transients occur on CPE side.

Lightning rarely strikes the phone line directly, but more commonly couples into the telephone line via several different mechanisms. One is that it strikes the high-voltage distribution lines on the same pole as the phone line. The strike may deliver a brief 1 kA pulse down a hundred meters or more of power line before arcing to ground through the nearest power-distribution lightning arrestor. Since the strike current runs parallel to the telephone lines, its very high dI/dt induces a large common-mode voltage in the parallel phone cable. For example, if the lightning strike delivers 100 A/µs di/dt (1 kA over a 10 µs rise time) down a 100 µH power-line inductance (say a 100 m power line at 1 µH/m), this generates a 10 kV inductive voltage down the power line. If the phone cable is relatively close (e.g. 10 m) to the power line compared to the coupling length (e.g. 100 m), then a large percentage of this inductive voltage will couple to the twisted pairs in the telephone cable below. Although the twisted-pair phone cable has a conductive sheath around it that is grounded periodically and that acts as an eddy-current shield, its efficacy is limited by its own return inductance and resistance through the ground path, which is often even further away than the inducing power lines. In other words, the power lines and the telephone cable form a very low impedance pulse transformer that may couple to the telephone line up to 30 or 50 % of the

lightning voltage drop down the power line. The net effect is that several kV of longitudinal transients can be put on the telephone line for any lightning strike on the power line that runs above the same telephone lines. Since the phone line may run for several miles, it may not be unlikely that a strike above it happens several times every lightning season.

Another coupling method for lightning is via ground-return bounce. Since the lightning strike must return to ground and especially if the ground is resistive, the local voltage at the ground return may bounce by thousands of volts for several tens of microseconds. If the local ground is at the switch end of the telephone line, of course this will induce a common-mode transient toward the CPE end of several kV. Conversely, if the strike ground return is local to the CPE, it will make the local ground bounce by several kV relative to the telephone switch end that may be miles away. Either mechanism generates a longitudinal transient between the telephone line and the local ground of several kV.

Lightning is not the only source of such transients. The power-distribution system can also generate common-mode induction transients through the same coupling mechanism. These transients may arise from power-distribution switching or heavy-duty loads (industrial motors, etc.). Generally, these induction events are rare, and are mostly a source of common-mode noise, not producing voltages high enough to cause damage.

These transients are the reason why telephone lines all have primary lightning arrestors to local ground at the PSTN (Public Switched Telephone Network) network access port. Normally, there is one primary arrestor on each side of the telephone line to a local ground, typically a clamp on a water pipe or ground stake. These arrestors trigger in the 300 to 600 V range. Common arrestors have been 6-mil carbon gaps, gas tubes, MOVs (Metal Oxide Varistors), or semiconductor breakover diodes. The carbon gaps and gas-tube arrestors are slow and may take several µs to trigger, allowing up to several kV for a few µs. Typically, the arrestors can withstand at least a 100 A surge for a standard lightning surge pulse of several hundred µs. The resistance of the telephone line limits the current. Typical 26-gauge twisted-pair cable has a resistance of 40 Ω per kft. Surge suppressors either have breakover characteristics where their forward voltages drop to a few volts when triggered but need at least 100 mA to keep them conductive, or have Zener voltage clamp characteristics. Voltage clamps (MOVs are the common example) need to be able to absorb many Joules of energy without damage (1 kV x 100 A x 100 µs = 10 J). With the breakover diode, the peak current may be several times higher because it provides little blocking voltage, but it dissipates less than 1/100th of the energy of voltage clamp because of its low forward voltage. The bulk of the surge energy is dissipated down the series resistance of the telephone line.

If the primary arrestors always were in place and properly grounded, then much of the observed lightning damage to DAAs would not occur. Unfortunately, over the life of telephone line, a number of ground connections at the network-access point may get disconnected due to building construction. The ground is often not reconnected because the telephone line works fine without it. The surge arrestors may also be damaged and not replaced, or the network-access port is removed and not replaced. Even a properly installed ground stake in a desert climate may fail if the soil dries out, thus causing a high-impedance return path to ground.

Arcing across the isolation barrier is the more serious DAA failure that arises when the primary arrestor protection is defective. Longitudinal voltages need to rise above 2 to 3 kV before arcing occurs. Lower voltages usually don't arc since most DAAs are designed to withstand transients of at least 1.5 kV and the continuous application of 1 kV_{RMS}. Even though longitudinal transients above 5 kV may be rare, electrostatic (ESD) transients can easily exceed 10 or 15 kV. A telephone product that includes a DAA might be struck by an ESD event and not have an adequate ground return. The resulting ESD event may then arc across the isolation barrier. For example, a user might be installing a fax machine at home and then plug the telephone line before plugging the power cord. If an ESD transient strikes while the fax machine is unplugged, then the DAA might be damaged due to arcing across its isolation.

There are several remedies for the ESD event. One is the use of common-mode, high voltage EMI capacitors between the chassis ground and the phone line. These are typically installed for reduction of EMI radiation and susceptibility. If each of these is around 470 pF, they will divide the voltage of an ESD transient by as much as ten times. Since these capacitors must meet the telephone-line isolation requirements, they will naturally withstand the divided voltage.

The IA3222/3223 chipset does not need these costly EMI capacitors because of the high RF impedance of the isolation capacitors. These capacitors achieve an effective breakdown voltage in the tens of kV at only the cost of the PCB area they occupy. In practice, excessive common-mode voltage will arc across the surface of the board. If the DAA designer doesn't select a preferred path for common-mode arcing, the surge will find its own path with consequent damage. A preferred arc path would normally be between either Tip or Ring and the chassis ground of the telephone product. The desired arc gap should be both shorter and more pointed than any other potential arc path. If part of the arc gap is on the circuit board it is important that the ends not have insulating silkscreen over them. For most worldwide applications, the gap should be at least 2.5 mm. This means that the other creepage (surface distance) distances should be at least 3 mm.

Metallic (differential) surges arise from the longitudinal lightning surges causing either the asymmetric triggering of the primary arrestors, or arcing of only one side of the line to ground (if only one primary arrestor is functioning). To protect against metallic surges, a DAA uses a surge suppressor that clamps the differential voltage to prevent damage. Good solutions provide surge immunity for both on-hook and off-hook DAA states. Protecting the off-hook state requires some form of current limiting to protect the off-hook path during the surge. Breakover diodes generally work better since they collapse the surge voltage, thus reducing the energy dissipated in the off-hook circuit over 100 times. MOVs can be used for surges, but because of their nearly two-to-one spread between minimum and maximum clamp voltages, the hook switch must be capable of withstanding much higher peak voltages than with breakover diodes. In addition, the hook circuit must turn itself off (blanking) during the surge in order to prevent excess dissipation.

Because the primary arrestors are not typically in a mutually triggered pair (unlike some gas tubes) during a common mode high voltage transient, one arrestor will always fire before the other. Ironically, on a telephone product with a breakover secondary surge protection diode between tip & ring, this can lead to overstress of this diode especially if the primary arrestors have a breakover characteristic (carbon gap, gas tube, or semiconductor breakover diode). The reason is that once a primary arrestor triggers on one side of the line, the longitudinal surge becomes metallic. This triggers the secondary breakover diode in the telephone product. At that point the other primary arrestor won't trigger at all, since there is now a low-voltage path around it through the secondary protector and back though the first primary protector that fired. In this situation, the breakover diode sees the same current as the primary arrestor. Typically, for this mechanism to occur both primary and secondary surge protectors need to have break-over characteristics.

There are several remedies to prevent this. One is to insert a resistance of about 5 Ω in series with Tip and Ring but before the breakover diode. The added resistance increases the voltage drop sufficiently to ensure that the second primary arrestor triggers on large current transients. Small transients can be absorbed by the breakover diode. If a resistor is used, it must be capable of withstanding the worse-case surge. If it has suitable fuse characteristics and is flame proof, then it can be used as an inexpensive slow-blow fuse for protection against line cross. Contact Silicon Labs for possible resistor types. Another remedy is to use a larger secondary breakover diode.

What surge capacity, then, does a breakover diode need to withstand for low field return rates? Experience shows that a DAA that survives an FCC part 68 Type-B surge provides good field immunity against most lightning surges over the life of the product. This surge specifies a 1 kV peak produced by discharging a 20 µF source capacitor with about 40 Ω of resistance for limiting current. Into a break-over diode, this produces a peak current of about 25A. Several vendors produce breakover diodes rated to survive this test. Although the designer can use more robust components to survive a FCC part 68 Type-A surge, (800V, 100A), the added expense is probably not warranted. Furthermore, a Type-A surge only requires a safe failure mode, not continued product operation. Generally, lightning surges that produce differential surges of 100A are likely to cause extensive damage to a wide variety of electrical devices in the house. As pointed out earlier, the telephone line resistance limits the peak current. Long lines will tend to have higher-voltage and more numerous surges, but the increased resistance helps limit the surge current.

The IA3222 Line Side has a smart power-limiting hook control circuit that prevents damage to the hook switch; either during high voltage surges or even if continuous high voltage is present on the line. The chip senses both line voltage and line current. If the line voltage exceeds 100V or the loop current exceeds 170mA, the hook switch turns off to prevent excessive power dissipation in the main hook transistors. This prevents thermal overstress damage as might occur during ringing peaks, from any surge voltage, or by connecting the DAA to a digital PBX supply with no current limit.

The digital PBX issue has been a major return rate problem on modem DAAs especially for laptop computers. Digital PBX phone systems normally provide 24 to 50V to power smart phones. This power may be current limited to 1A or even more, only to prevent a fire hazard. Some systems provide power, control and audio digital signaling down the normal Tip and Ring pair. If a regular telephone device is plugged into these lines, it may damage the DAA, since normal DAAs only expect up to 120 mA of loop current.

Power-Line Cross

A power-line cross happens when a power line erroneously gets connected to the phone line. All DAAs provide isolation protection against common-mode power line cross, but may not provide protection against differential line cross (full power applied between tip and ring). Most regulatory standards only require protection against common-mode power-line AC voltages and not differential power line voltages. Line cross is a much rarer event than lightning surges. Over the life of the product, this typically has less than a 1% chance of happening.

A line cross can occur from the user side or from the telephone system side. If the chassis of a telephone product somehow gets shorted to one side of the AC power line, then the DAA isolation protects telephone-company technicians and equipment from

excessive voltages and power. From the telephone system side, a line cross might occur if a power line falls across the telephone line shorting to one side of the line. Power-line cross is different than lightning surges because of its longer duration. This makes it much more dangerous even though it is less likely than lightning surges. Failure can occur either from isolation breakdown or from consequent excessive voltage between Tip and Ring, which can create a fire hazard in the DAA.

A power-line cross may start out as a longitudinal high-voltage event but may quickly turn into a metallic event. When a power line gets connected to one side or the other of the telephone line, it may cause the primary surge suppressor to trigger, which in turn burns open, leaving the AC mains on one side of the phone line. Then, either if the telephone device goes off hook, or if the breakover diode triggers, the other primary arrestor may trigger, creating a path directly through the DAA for the AC power line. In this scenario, there may be very little telephone line resistance in the current loop (less than 50 m of line) to limit the current. The result is a destructive failure of the DAA. It may burst into flames due to continuous pouring of energy into the DAA surge suppressor, which is normally not capable of continuous currents above 1A.

Safe differential line-crossing failure, when required, only means that the product needs to fail safely on a line cross, i.e. not burst into flames during the test. Designing a DAA to survive a line cross is possible but at a significant cost. The simple method is to use an expensive 600 V_{AC} PTC (Positive Temperature Coefficient) resetable fuse.

If the DAA needs to provide safe differential line-crossing failure, the normal solution is to have some type of slow fusible link. Fast-blow fuses will likely get blown by lightning transients and are therefore not recommended. There also exist special (and costly) telecom fuses that will survive a 25A peak Type B surge but will blow on a differential line cross event. Another solution is to use a 5 to 10 Ω, 1 to 2 W, flame-proof metal-oxide resistor for a fusible link. With some testing and care, this cheaper solution will withstand the Type B surge but safely blow on a line-crossing event. (Contact Silicon Labs for possible resistor types.) This also has the advantage of limiting the surge current that results from asymmetrical firing of the primary lightning arrestors. Any fusible link needs to be flame proof and physically separate from the PC board, since the UL 1459 test ramps the AC voltage slowly up to 600 V_{AC} to allow components to generate heat and possibly start a fire, rather than just blow apart. If a component such as a metal oxide resistor begins to glow and is lying flat on the PC board, it will carbonize the PC board material, which may lead to conductive tracking (carbonized insulator becoming conductive) and possibly fire.

Common-Mode Noise from the Mains Supply

A hidden common-mode noise issue arises from the absence of the third (green) wire safety ground in home AC power wiring. In the US, third-wire grounds and three-prong AC outlets were not installed extensively until the mid-1950's and were not required by code until the early 1960's. Europe and other countries have similar histories. Thus in older homes third-wire grounds are missing in some or all rooms, even if three-prong sockets are present. When computer equipment with switching supplies is plugged into such an outlet, up to half of the AC mains voltage can be measured on the chassis ground relative to real earth ground (or the telephone) line. The reason is that most computer switching supplies have pi network power-line EMI filters that have RF decoupling capacitors in the nF range tied between live, neutral and ground. If the third-wire ground is not actually grounded, the capacitors in the filter create a divider between live and neutral with the third-wire ground. It is possible to get a slight electrical shock from a computer chassis just from this effect. More significantly, it creates a very large common-mode noise voltage between the phone line (in effect a ground connection) and the local, ungrounded ground wiring.

This large AC common-mode voltage sometimes causes overload problems on resistor-capacitor isolated Caller ID circuits. The IAI3222 does not have this issue since it is completely isolated. Even with otherwise isolated DAAs, EMI immunity capacitors, if mismatched, can introduce noise on the telephone line, especially if large AC line transients are present. For example, if two 470 pF EMI capacitors are mismatched by 5%, the 23.5 pF unbalance has an impedance of 2.3 MΩ at 3 kHz. Against a typical line impedance of 600 Ω, this represents 72 dB of common-mode balance. If the power line has 20 V audio-band transients and the third wire ground is disconnected, this results in 10V at the chassis and will inject about 2.6 mV of audio noise on the phone line, enough to disrupt most high-speed (V.90, V.34, V.32) modem communication. For this reason, EMI bypass capacitors, when they are necessary, should be of the lowest value necessary to reduce EMI to the desired level.

Worse yet, some capacitively-coupled DAAs use more than 60 pF of signal-isolation capacitance that is not balanced relative to Tip and Ring. Even without EMI capacitors, significant noise can be injected into the line if the system third-wire ground is floating. Similarly, base-band linear opto-isolated DAAs can inject line noise even though the capacitive coupling across the isolation barrier may be less than 1 pF. The reason is that opto-isolated systems need a gain of almost 100 on the transfer and servo photodiodes because of the typical 1 % current-transfer ratio. Normally, there is a small amount of isolation capacitance in the sensitive servo or transfer photodiode to the effect that at 3 kHz the common-mode balance may be 80dB or less.

EMC

Another key advantage of the IA3222/3223 chipset is that many applications do not require the usual telephone-line EMC suppression components. The 2 pF total value of the isolation capacitors presents significant impedance at VHF and UHF radiating frequencies. At 300 MHz, 2 pF has a reactive impedance of 265 ohms— comparable to that of ferrite beads. This coupling impedance is significantly higher than other capacitor DAAs where the isolation impedances can be ten times lower or even less. Compared to these other DAAs, the chipset will couple better than 20 dB less RF to the phone line if no other RF suppression is used and will be comparable to the other capacitor-coupled DAAs where ferrite beads are used.

If higher levels of RF suppression are required, adding EMI shunt capacitors between each side of the line to the chassis will be more effective than adding ferrite beads. To minimize the need for EMI shunt capacitors, the line side area (antenna) should be minimized and placed as close as possible to the phone line connector. Extending the chassis ground on each of line side (while still maintaining minimum isolation creepage) will act as an RF shield. If board area is available, the EMI line capacitors can be fabricated like the PCB isolation capacitors by using the upper and lower PCB layers. Matched 10 pF capacitors on each side of the line to the chassis would attenuate line RF by about 20 db.

RF Susceptibility

For DAAs, large common-mode RF signals below 2 MHz can be a serious source of interference. In particular, AM radio-band transmitters in the 500 kHz to 1.6 MHz range are common in urban areas. Although the field strength for AM radio is typically no more than other urban signals (TV, FM, two-way radio, cell phones, etc.), the twisted-pair telephone line from the pole plus the unshielded telephone line in the building makes an excellent long-wave antenna since neither of these are shielded like the multi-pair cable on the pole. Because of the long wavelengths in this band (150 to 600 m), a quarter-wave long wire antenna has a large RF capture area, providing up to a hundred times higher common-mode signal levels than the field strength per meter. Consequently, it is not unusual to see many Volts of common-mode RF signal on the telephone line. This can easily be seen by putting an oscilloscope probe on tip or ring. To prevent interference from these AM-band signals, some DAAs require both expensive series inductors in the range of several µH and high-voltage shunt capacitors.

Without the need for these costly RF suppression components, the IA3222/3223 chipset achieves very high common-mode RF immunity. This results from the combination of very low isolation capacitance and internal filtering. Typically, RF immunity of the IA3222/3223 will be sufficient and the DAA will perform quite well without any special RF suppression components. On the other hand, if immunity is desired to the level specified in EN 55024 or even to Brazil's more demanding Anexo a Resolução No 237, a pair of 470 pF high-voltage capacitors between Tip/Ring and the chassis ground is normally sufficient. In general, filtering components work both ways: any RF solution that works well for radiated signals will work well for susceptibility in the same frequency range.

RETURN LOSS AND TRANS-HYBRID RETURN LOSS

Telephone devices transmit and receive bi-directionally down a twisted-pair line. All of the transmitted signal would be present on the receiver were it not for a cancellation circuit called hybrid or two-to-four-wire hybrid. A hybrid works by canceling the actual echo back from the line with the expected transmitted reflection. The expected reflection is determined by applying the transmitted signal through an analog of the driver impedance applied across an analog of the line impedance (also called a “line mirror” short for “line-mirrored impedance” or “balance network”). If the actual line impedance and drive impedance is identical or balanced perfectly by the line mirror and mirror drive impedance, then the echo cancellation will be complete. In practice, the impedance varies significantly with the length of the line and with the presence of bridged taps (parallel open-circuit twisted pair stubs), so that echo cancellation varies with the frequency of the transmitted signal and with the line.

The standard measure of the cancellation of the hybrid balance is return loss. This is a measure of the reflection from the transmit path back to the receive path in terms of loss (attenuation) normalized to levels on the telephone line and expressed in dB. The higher the loss, the lower the reflection and the better the hybrid balance. For example, a 20 dB return loss at a given frequency indicates that the transmitted signal at the receiver will be 20 dB lower than if the same level of signal was received on the telephone line from an outside source. Return loss for a line and its terminating impedance can also be calculated if both impedances are known.

Hybrids are normally present both at the SLIC or switch end and at the CPE or loop termination end. Confusion sometimes arises since return loss is used to measure both the accuracy of the impedance termination on either end of the phone line and also to measure the efficacy of the hybrid in cancelling the reflection. This latter is called trans-hybrid or four-wire return loss. The return-loss figure on the termination impedance indicates the reflected signal amplitude due to the impedance mismatch from an ideal termination.

Many telephone line interfaces, whether SLIC or DAA, may provide several levels of hybrid balancing. Commonly, a first-order analog compromise line mirror is used, which may provide only about 10 dB of balance over a range of telephone lines. Its purpose is to reduce the dynamic range of the receiver channel (or codec) by this amount since telephone systems require about 80 dB of dynamic range. If the application requires better hybrid balancing, then some form of dynamic or line calibration is required.

The degree of total hybrid balancing needed is a function of the telephone application. The main purpose of Central Office or End Office hybrid balancing is to reduce far-end voice echoes that can be very annoying and degrade the quality of service. Surface communication paths (optical fiber, coax, etc.) round-trip echoes between the North American West Coast and Europe can approach 200ms. On a new line installation, the hybrid mirror at the Central Office requires tuning at least for loaded versus non-loaded lines. Telephone-network echo cancellers dynamically adjust hybrid balance, but in order to work best require some minimum compromise hybrid balance. Central Office hybrid tuning assumes that the telephone line is terminated with a standard impedance. For most of the world this is 600 Ω. In some countries, the 600 Ω impedance is replaced with an RC network that better approximates the complex impedance of a long non-loaded telephone line. This reduces hybrid-balancing differences between short and long lines.

In practice, the return-loss matching of the terminating impedance is not very critical for two reasons. First, the bi-directional loss down a typical telephone line reduces the effects of any 600 Ω or complex impedance mismatch by twice the nominal loss. For example, since the average telephone line loss is about 4dB, on such a line the effects of a termination mismatch on the Central Office SLIC hybrid balance will be reduced by 8 dB (the attenuation in each direction). Secondly, the line-length variation of the return loss is the dominant effect, swamping most production termination impedance variations. For example, a median-length telephone line of 5,000 ft has an added 400 Ω of series resistance and a distributed capacitance of around 80 nF. Since most speech audio is below 1 kHz, the telephone-line resistance has the dominant effect on echo that is not mitigated much by the distributed capacitance. Evidence that termination impedance variation is not critical is suggested by very wide margins on return loss requirements in mainstream regulatory approval. US FCC Part 68 has no return-loss impedance requirement, that of TBR21 is very low (only 8 dB) and JATE requires only a few dB.

On the CPE side of the telephone line, there is no regulatory requirement for trans-hybrid return loss, but that parameter has a more significant functional impact on modem performance or audio quality.

All high-speed full-duplex modems (V.32, V.34, V.90 and V.92) during training build an exact line mirror (of what is left over from the DAA compromise hybrid) to cancel the echo to better than 70 dB. The IA3222 has a compromise trans-hybrid balance network on the Line Side that improves the dynamic range performance of the analog channel by minimizing the transmitted noise and distortion reflected back into the receiver channel. Both of these are very critical for high-speed modems. A hidden critical element for high-speed modems is hybrid thermal drift. If the hybrid return loss, transmitter or receiver gain drifts by even a small amount (less than -60 dB) between initial training and several minutes later, the modem performance can be greatly degraded since the un-

cancelled residual is seen as noise. Trans-hybrid drift mostly arises from thermal effects due to heating of the Line Side both from the line current and the electronic environment. The IA3222 was designed to have very low thermal drift to minimize these effects.

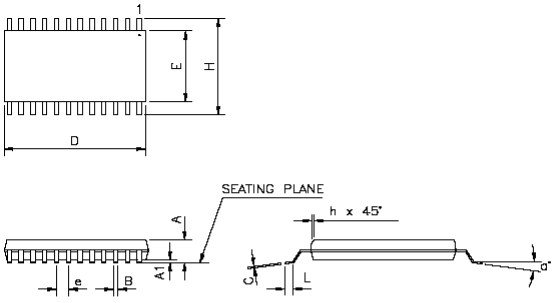
In telephony applications, hybrid return loss is heard as “sidetone”. Some sidetone is desirable as long as it is not excessive in volume. The IA3222 hybrid network, like most telephones, provides a good compromise sidetone over most normal loaded and non-loaded lines without requiring other compensation networks.

Better trans-hybrid balance against any line can be achieved by adding a suitable analog or digital transform between the transmitted audio and the received signal summing node. This can be done in the analog domain with RC networks, some type of receiver summing node (either resistive or using an op amp) and some type of transmitter inversion.

Similarly, different termination impedances can by synthesized either in the analog or digital domain by complex transformation of the receiver signal back into the transmitter input. In some digital DAAs, the sampling delay prevents this except for very low frequencies. But since the IA3222/3223 uses eight-times oversampling, line to Rx pin and Tx pin to line delays are significantly less, thus making impedance synthesis possible.

PACKAGE INFORMATION

QSOP-16 and QSOP-20 Packages

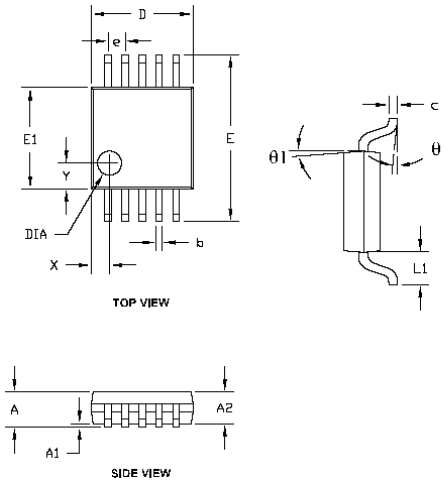


JEDEC #	MO-137AB		MO-137AD	
TYPE	16 LEAD		20 LEAD	
SYMBOL	Min	Max	Min	Max
A	0.060	0.068	0.060	0.068
A1	0.004	0.008	0.004	0.008
B	0.009	0.012	0.009	0.012
C	0.007	0.010	0.007	0.010
D	0.188	0.197	0.337	0.344
E	0.150	0.157	0.150	0.157
e	0.025 BSC		0.025 BSC	
H	0.230	0.244	0.230	0.244
h	0.010	0.016	0.010	0.016
L	0.016	0.035	0.016	0.035
α°	0°	8°	0°	8°

NOTES

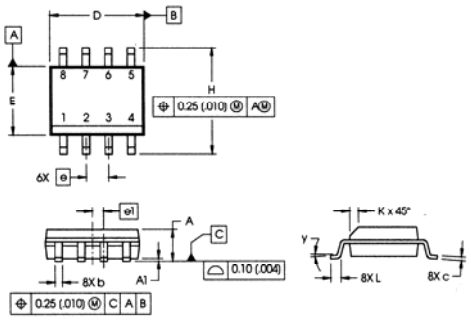
1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. DIMENSIONS ARE GIVEN IN INCHES.
5. LEAD COPLANARITY IS 0.003 INCH MAX.

MSOP-10 Package



SYMBOL	INCHES		
	MIN	MAX	ACTUAL
A	0.036	0.043	0.038
A1	0.002	0.006	0.004
A2	0.032	0.037	0.034
b	0.007	0.010	0.008
c	0.003	0.009	0.006
D	0.116	0.120	0.118
E	0.190	0.198	0.194
E1	0.116	0.120	0.118
e		0.020	
L1	0.036	0.040	0.038
θ	0°	8°	5°
θ1	5°	10°	7°
DIA	ø0.028 depth=0.004		
X	0.017	0.025	0.021
Y	0.026	0.034	0.030

SOIC-8 Package *(JEDEC Outline MS-012AA)*



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

ORDERING INFORMATION

IA3222/IA3223 DAA Chipset with Analog Interface

DESCRIPTION	ORDERING NUMBER
IA3222A – Line Side US/Japan DAA IC	IA3222A-IC CB8
IA3222B – Line Side Enhanced Worldwide DAA IC	IA3222B-IC CD10
IA3223 – System Side Worldwide DAA IC	IA3223-IC CI16
IA3223A – System Side Worldwide DAA IC with pin hook control	IA3223A-IC CI20

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